DOI:10.22413/ijatest/2021/v6/i3/7

Analysis of CMOS 45nm Transmission Gate based Pulsed Latch

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Abstract: ***Pulsed latches are becoming more popular . By combining latch and flip-flop features, they can provide an appropriate sequential element with superior performance, area, and low power consumption. Despite the fact that circuit reliability and robustness against voltage, and temperature variations are key issues in today's technology solutions, no substantial reliability study for pulsed latch circuits has indeed been proposed. The goal of this paper is to look into the effect of different VT variations upon on behavior of pulsed latches, taking both the pulser and the latch into account. Furthermore, a transmission gate design approach is presented to improve the reliability of pulsed latch circuits while retaining their primary benefits of high performance, low power consumption, and small size. Experiments with Tanner EDA CMOS 45nm demonstrate the proposed approach's ability to maintain the same level of reliability across a wide range of supply voltages and temperatures while requiring very little area overhead.***

Keywords: Tanner EDA, CMOS 45nm, Latch, transmission gate

I. INTRODUCTION

In traditional ASIC designs, flip-flops are the most frequently used sequential element. This is because their timing model is simple, which simplifies the process of designing and verifying timing. Master-Slave Flip-Flops (MSFFs) are the most common and traditional implementations of flip-flops due to their reliable operation and simple timing characteristics. However, so because MSFF microarchitecture is frequently implemented utilizing two sequential latches, it's indeed time, power, and space inefficient. As shown in Figure 1.1, a typical MSFF. [1]

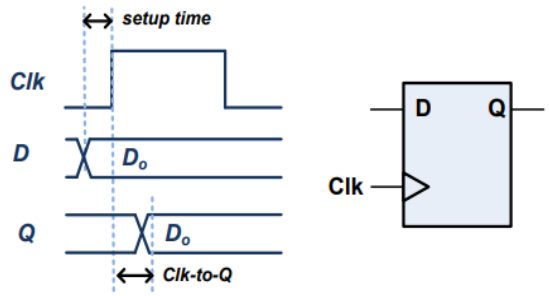

Fig.1. A simple schematic depicting a master-slave flip-usual flop's timing overhead.

On several occasions, pulsed latches have been proposed as a more efficient sequential element implementation than flip-flops. Pulsed latches are latches that are driven by short pulses generated by a pulser circuit from a conventional clock signal. Pulsed latches have a lower timing overhead and consume less power than flip-flops. Additionally, because the latch is significantly smaller than the flip-flop, significant area savings can be expected when a single pulser is shared by multiple latches. Additionally, novel methods for increasing the dependability of pulsed latches without sacrificing performance, area, or power must be developed. In addition to being used in logic routes, sequential components are occasionally used to create register files for data storage. While flip-flops and latches are frequently used in certain applications, pulsed latches may be a more attractive alternative. By utilizing pulsed latches, it is possible to reduce the size of the register file while reducing latency and power consumption. However, it must be compared to commonly used SRAM-based register files. Along with single-read and single-write register files, which are common in most designs, multiport register files are especially advantageous for a limited number of applications. On the other hand, the conventional method of creating multiport register files incurs significant overhead in terms of space, power, and performance. Due to their versatility, pulsed latches can be an attractive and more efficient alternative implementation of multiport register files.[2,3].

We begin by comparing the performance of a latch implemented in GDI, static CMOS, and transmission logic. By comparing the implementation of these techniques, it was determined that a pulsed latch circuit could be implemented using a transmission gate.

The second section discusses the literature survey. Section III discusses various techniques for implementing D-latch. Section IV discusses the transmission gate pulsed latch that is proposed for 45nm CMOS technology under supply voltage scaling. Section V discusses the findings.

. Finally, section VI draws some conclusions.

II. LITERATURE SURVEY

Pulsed latches have long been proposed as a way to reduce power consumption while increasing performance. [4] employed PLs with fairly wide pulse widths to enable cycle lending and to tolerate clock skew. [5] demonstrated the use of PLs as the primary sequential elements to enhance the effectiveness of the Intel XScale microprocessor without requiring excessive clock power.

Baumann et al. [6] suggested three strategies for selectively replacing MSFFs with PLs in order to boost the ARM926 microprocessor's performance. However, due to the buffer insertion, some area as well as power overhead were introduced. Baumann et al. [7] implemented that PLs be used

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in place of MSFFs in an ARM microprocessor. This was done to achieve some performance gains that were then used as timing margins to account for within-die variations. [8] proposed a traditional pulser and a latch composed of a tri-state inverter and a static keeper. The effect of process variations on many pulsed flip-flops was discussed in [9], along with two techniques for mitigating that impact. However, the effect of voltage and temperature on the proposed techniques was not investigated, and the proposed approaches were not quantified in the presence of these two effects.

Dhong et al. [10] demonstrated a novel pulser design in which the output pulse width is measured by the dc voltage at the input of a NAND gate rather than the delay chain used in the TGPL's conventional pulser. In [11] and [12], energy, delay, and area comparisons were made between various flip-flop and pulsed latch classes and topologies. The study demonstrated that when energy, delay, and area tradeoffs are considered, TGPL is by far the most effective topology across a broad range of applications.

In [13] and [14], the impacts of PVT variations on various flip-flop and pulsed latch topologies were investigated. Additionally, the study demonstrated that TGPL exhibits the excellent efficiency and resilience to process variation. As demonstrated in previous research, TGPL, the architecture on which this paper will focus, is among the most attractive architectures for PL circuits. Even so, there are still a few challenges in the TGPL (and PL in general) design that must be overcome in order to provide reliable procedure under PVT variations.

III.IMPLEMENTATION OF D-LATCH USING VARIOUS TECHNIQUES

In this section a D-latch has been implemented using GDI, Transmission Gate, Static CMOS logics using Tanner EDA in CMOS 45nm technology. The general circuit of D-latch has been demonstrated in the Figure 2.

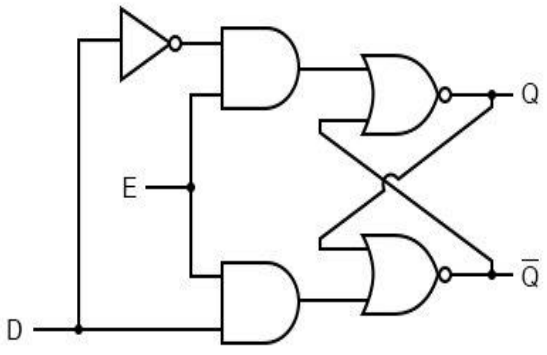

Fig.2. D Latch Implementation

a. Implementation using static CMOS Logic

The basic AND,NOR and Not gates are implemented using CMOS logic. Based on them D-latch has been implemented. The static CMOS implementations of AND,NOR and NOT gates are shown in Figures 3,4 and 5 respectively.

The CMOS AND gate produces the output as '1' only when the inputs "A" and "B" are high which mean the NMOS transistors M1,M3 and PMOS transistor M6 are ON. In all other remaining cases the outputs are low.

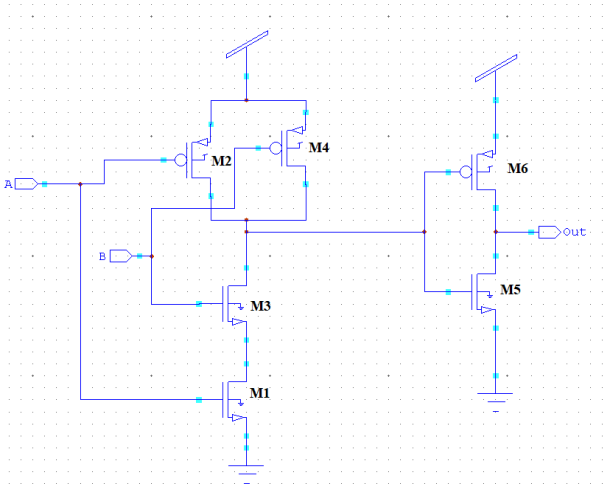

Fig.3. CMOS AND Gate

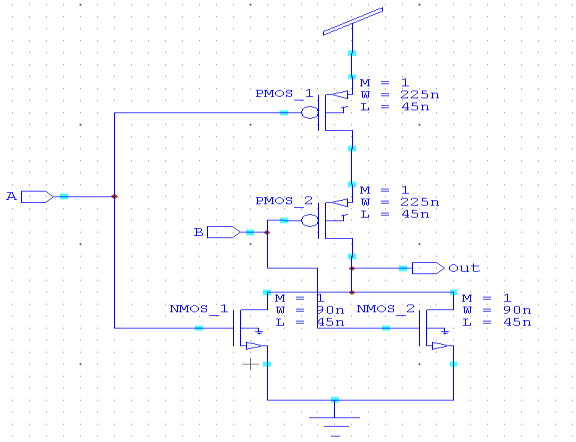

Fig.4. CMOS implementation of NOR gate

The NOR gate produces the output as high when both PMOS transistors are ON with inputs A and B are low. In all other cases the outputs are low.

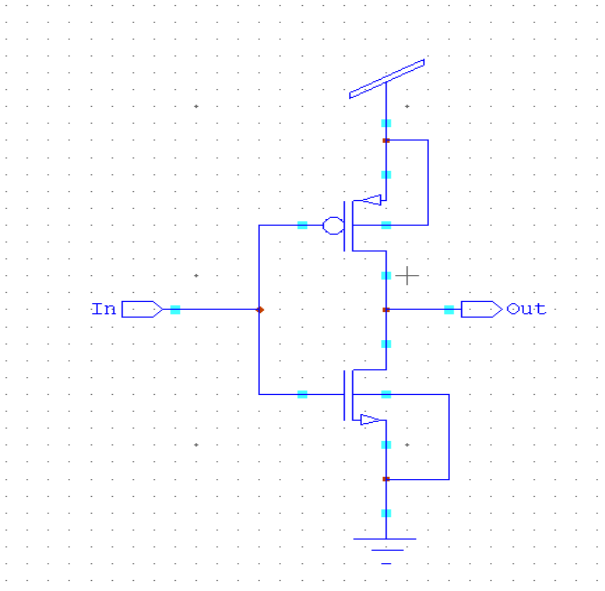

Fig.5. CMOS implementation of NOT gate

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The NOT gate output is inversion of the input. If the input is high then output is low else if the input is low then output is high.

b. GDI Logic Implementation

The basic AND,NOR and Not gates are implemented using GDI logic. Based on them D-latch has been implemented.

Gate diffusion input (GDI) is a technique that is used in place of static CMOS logic. The main difference between CMOS and GDI is that, even in GDI, the allocation of supply and ground to pMOS and nMOS is not fixed. Two transistors are required to perform two distinct and complicated logic operations. As a result, it's a less transistor-intensive circuit, and the basic GDI circuit will save power due to its logic flexibility. Throughout comparative analysis with static CMOS-based circuits, GDI-based digital circuits consume less power, have a faster response time, and take up less space[15,16].

3.1. GDI based AND Gate

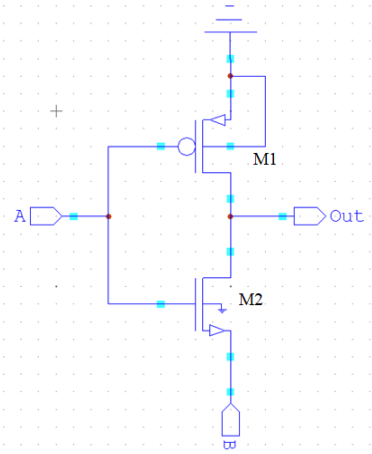

Fig.6. GDI technique dependent AND gate

Figure 6 illustrates the AND gate by using GDI method. It consists of 2 M1 as well as M2 transistors, with either A input connected both to the M1 as well as M2 transistors' gate terminals. The B input is connected to the M2 transistor's source, whereas the M1 transistor's supply is connected to ground. To evaluate the output logic, the drains of M1 and M2 have been connected together.

3.2 GDI based OR gate

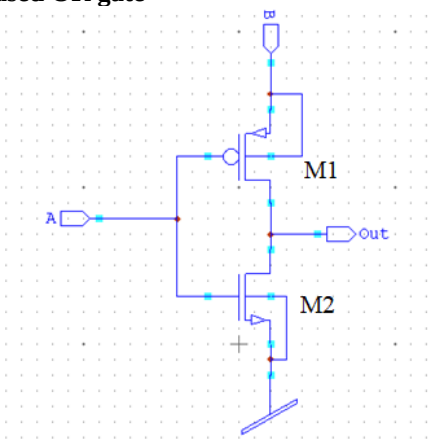

Fig.7. GDI technique dependent OR gate

The OR gate depending on the GDI mechanism is illustrated in Figure 7. It comprises of 2 M1 as well as M2 transistors, with both M1 and M2 transistors' gate terminals connected to a input. The transistor's source M1 is connected to input B, even as source M2 is attached to VDD. The drains of M1 and M2 are connected together to confirm the performance rationale.

C. D- Latch using Transmission Gate

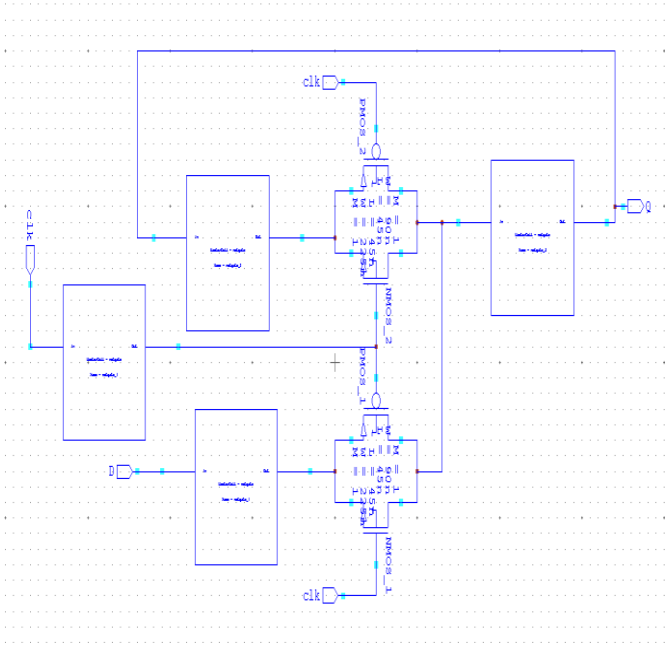

Fig.8. D-latch using Transmission Logic

In the figure 8, the D-latch is designed using two transmission gates and 4 NOT gates. When the clk/en signal is high the output follows the input and when clk/en signal is low the output remains as in the case of previous state.

d. Comparison of D-latch using different technologies

The D-latch is implemented in Transmission gate logic,GDI logic and static CMOS logic technologies. The comparative analysis of these is analysed in terms of area, power and speed.

	CMOS	GDI	TG
NUMBER OF TRANSISTORS	22	10	10
POWER (W)	$8.7910*10^{-8}$	$2.02*10^{-8}$	$5.808*10^{-8}$
DELAY (s)	$301.8481*10^{-12}$	$54.23*10^{-12}$	$48.356*10^{-12}$

Table 1: comparison of D-latch w.r.t various technologies

From the table I it is evident that GDI logic is consuming low power with less number of transistors but delay is lesser in transmission gate technique.

IV. PULSED LATCHES AT THE CIRCUIT LEVEL

The transmission gate was chosen for implementation based on the implementation of D-latch and the comparative analysis in Table 1. Tanner EDA is used to implement the circuit in 45nm CMOS technology. Figure 9 illustrates our suggested pulser self-gating technique. Each latch

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necessitates three additional transistors in addition to the single pull up transistor required for each pulser circuit. Two of the latch's three additional transistors function as simple comparators, comparing the latch's input and output values (the transistor on the right compares the input D to the inverted value of the output (Qbar), while the transistor on the left wants to compare the inverted value of the input to an internal node storing the same output value). If the input and output values seem to be identical, a few of these two transistors are on with one side set to logic '0,' thereby lowering the EN signal to logic '0.' If the input logic value is different than the output logic value, one of these two transistors would then turn on with one side at logic '1', pulling the EN to a weak logic '1'. When the EN signal is logic '1', the third transistor with its gate connected to the EN signal is being used to discharge this same pre-charged Pulse Enable signal . This Pulse Enable signal is a wired-OR signal that is shared by all latches. As a result, whenever a latch's stored value needs to be modified, the pulser circuit is enabled by pulling down the Pulse Enable signal. The pull-up PMOS transistor is used to charge the common Pulse Enable node before it is activated by either the inverted pulse signal or a delayed version of the clock signal. This proposed methodology may be used alone or in conjunction with the traditional clock gating methodology to improve clock gating efficiency [17].

V. RESULTS

The D-latch transient analysis waveform has been depicted in Figure 9. If enable signal is high the output follows the input, if enable signal is low the previous state outputs will be next state outputs.

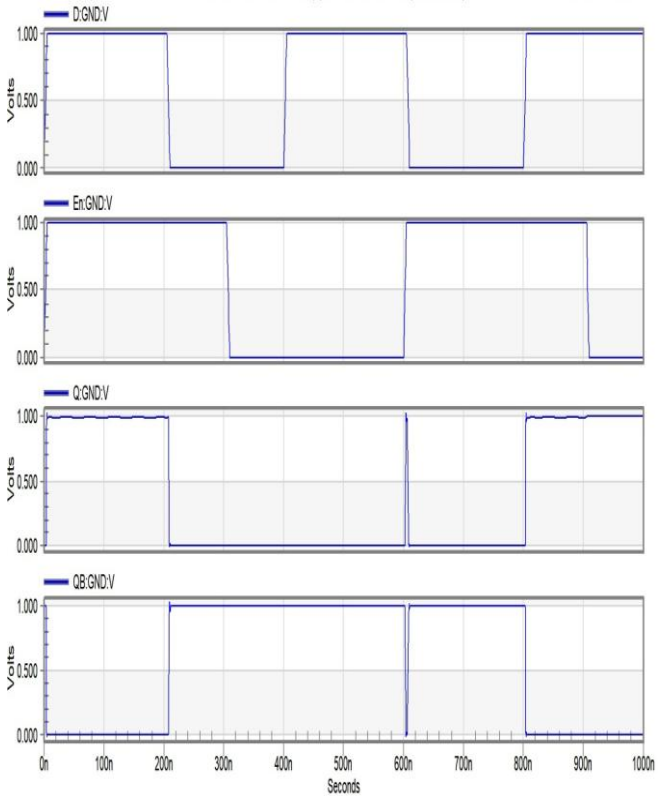

Fig.9. Transient waveforms of D-latch

Voltage-Temperature Analysis

TEMPERATURE	VDD= 1V	
	POWER (IN WATTS)	DELAY (s)
10	$2,77*10^{-5}$	$446.95*10^{-12}$
20	$2.56*10^{-5}$	$444.24*10^{-12}$
30	$2.37*10^{-5}$	$440.88*10^{-12}$
40	$2.2*10^{-5}$	$436.76*10^{-12}$
50	$2.05*10^{-5}$	$431.64*10^{-12}$

TEMPERATURES	VDD=0.7	
	POWER (IN WATTS)	DELAY (s)
10	$715*10^{-6}$	$2.66*10^{-9}$
20	$6.49*10^{-6}$	$0.1449*10^{-9}$
30	$5.9*10^{-6}$	$1.52*10^{-9}$
40	$5.31*10^{-6}$	$1.6*10^{-9}$
50	$4.91*10^{-6}$	$2.71*10^{-9}$

Table 2: PVT analysis of proposed Circuit

Because power consumption is an important metric for such circuits, any force overhead associated with the proposed technique should be kept to a minimum. At 1V and 0.7V ,50 deg C, the proposed circuit consumes less power. As the voltage reduces spped as well as power consumption also gets reduced, which is evident from table 2.Nonetheless, at this lower voltage, the standard PL register is more likely to disappoint, making its energy numbers useless. Moreover as the design is based on TG logic, it is evident that less number of gates will be used when compared with other techniques as depicted in table 1. From this it is concluded that the proposed circuit uses area and consumes low power and works with higher speed at lower voltages.

VI. CONCLUSION

In this paper, we investigated the effect of different VT variations on the behavior of pulsed latches, considering the effects on both the pulser and the latch. Furthermore, a transmission gate design method is adopted to ensure the efficiency of pulsed latch circuits while retaining their primary benefits of high performance, low power consumption, as well as small size. Experiments with Tanner EDA CMOS 45nm show that the proposed approach can maintain the same level of reliability across a wide range of supply voltages and temperatures while consuming very little area.

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