DESIGN OF SRAM MEMORY USING REVESIBLE AND GDI LOGICS

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Abstract: Power consumption is a critical issue in VLSI design. Reversible logic and GDI logic have gained popularity in recent years because to their low power consumption features. These logics have a wide range of uses in upcoming technologies. This logic is critical for the development of low-power structures that are required for the creation of arithmetic circuits used during quantum computing, nanotechnology, and other low-power designs. The GDI method is used to build a variety of reversible logic gates in this paper. A SRAM memory cell has been built utilizing the developed reversible logic gates for improved performance over current designs. Additionally, performance factors like as quantum latency and transistor count are examined for various SRAM designs. Tanner EDA Tools utilizing CMOS 45nm technology are used to simulate the process.
Keywords: Reversible logic gates, GDI logic, SRAM

I. INTRODUCTION

The increasing use of mobile phones as well as other handheld devices, along with the simplicity with which fast communication networks may be accessed, has led to a considerable rise in demand of audio and visual administrators on the system. One of these gadgets' main objectives is to build energy-efficient frameworks that allow longer battery life. Due to the increased handling and capacity requirements for these hand-held devices, high-resolution photography has worsened the problem of intensity usage. To be honest, embedded static random access memory (SRAM) alone accounts for about 30% of power usage [1]. Dynamic power consumption is linear with voltage, and memories are intended to run at extremely low voltages in order to gain substantial power savings during memory operations. [2]. While this presents a major hurdle to incorporating such memories into mainline processors, it is beneficial in processors intended for interactivity applications, that are known to just be error-tolerant [3].

Due to the rising need for more functionality at a reduced energy cost, high density and low-power designs have become increasingly critical for a wide variety of applications. With increasing need for greater memory capacity and speed, it has become essential to guarantee that control consumption is decreased and dependability is raised at a quicker rate for both individual memory cells and the memory framework as a whole.

Designers have faced many difficulties in the creation of conventional design components during the last few years.

The primary issue with these traditional methods is power dissipation, which is a critical component in today's integrated circuit designs. Because traditional circuits waste more power in VLSI design, reversible logic is a potential technology for addressing this issue owing to its inherent ability to reduce power dissipation. It has received significant research and implementation for VLSI architectures. It encompasses a variety of applications, including low-power CMOS, quantum computing, and nanotechnology. Additionally, reversible computing will result in an increase in the system's total energy efficiency.

Advances in reversible logic technology have aided in the performance enhancement of computer architectures. In this section, we compare the power, slew rate, and latency of several reversible logic gates in order to determine their potential uses in VLSI circuits.

Reversible logic circuits have an equivalent number of inputs & outputs as well as a one-to-one mappings between the input & output vectors; this guarantees that the input state vector is always recoverable from the output state vector. The main objectives of reversible circuit design are to reduce gate count, garbage outputs and quantum cost. Any reversible circuit must utilize as few reversible logic gates as feasible.

GDI (Gate Diffusion Input Method) - In[4], a new low-power modeling method was created to address a wide range of low-power issues. The GDI method enables the use of a broad range of dynamic combinational logic with just two transistors. This method is ideal for creating fast, low-power circuits by employing less transistors whilst enhancing power characteristics and enabling the creation of basic Shannon circuits utilizing theorems[4,5].

II. IMPLEMENTATION OF GDI LOGIC

Gate diffusion input (GDI) is used as a replacement to static CMOS logic. The primary distinction between CMOS and GDI is that even in GDI, the supply & ground allocation to pMOS & nMOS are not set. It just needs two transistors to execute two different and complex logic operations. As a result, this is a circuitry with less transistors, and the fundamental GDI circuit saves power due to logic flexibility. However, performance fluctuations occur as a consequence of threshold voltage drops[6,7].The three inputs in GDI are as follows:
• N- input to the nMOS source/drain • P- input to the pMOS source/drain

The straightforward digital gates (AND, OR, XOR) are designed to maximize swing. In comparison to static CMOS-based circuits, a GDI-based digital circuit uses less power, has a shorter latency, and occupies less space. In this part, basic logic gates are constructed using GDI technology and emulated using CMOS 45nm technology.
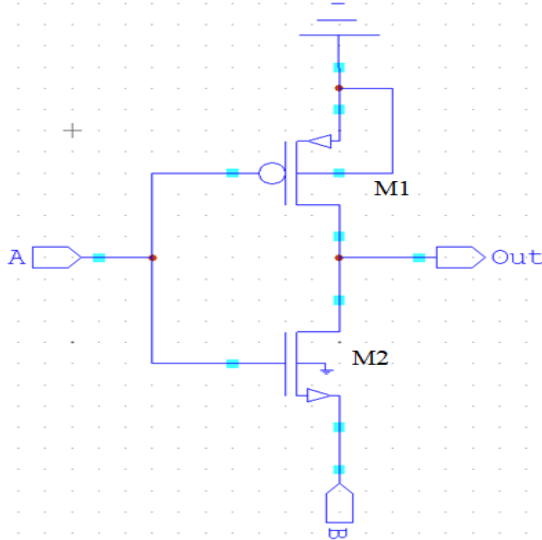
2.1 GDI based AND Gate

Fig.1. GDI technique dependent AND gate

The AND gate is shown in Figure 1 using the GDI method. It consists of two M1 and M2 transistors, with the A input linked to the gate terminals of both the M1 and M2 transistors. The B input is linked to the source of the M2 transistor, whereas the source of the M1 transistor is connected to ground. The drains of M1 and M2 are connected together to assess the output logic.
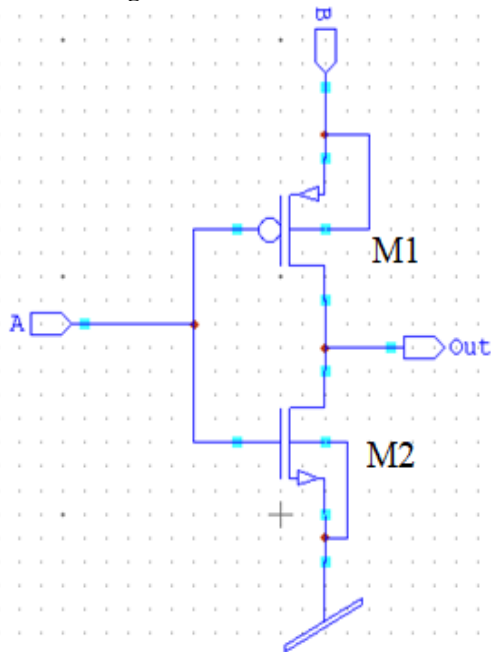
2.2 GDI based OR gate

Fig.2. GDI technique dependent OR gate

Figure 2 illustrates the OR gate based on the GDI method. It comprises of two M1 and M2 transistors, with the gate terminals of both the M1 and M2 transistors connected to the A input. Input B is connected to the transistor's source M1, while source M2 is connected to VDD. To verify the performance rationale, the drains of M1 and M2 are linked together.
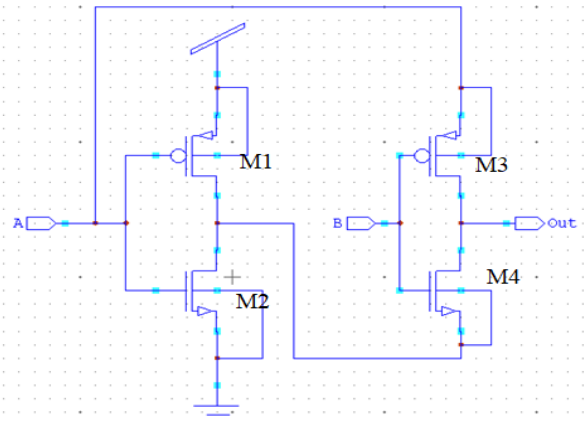
2.3 GDI based XOR gate

Fig.3. GDI based XOR gate

Figure 3 illustrates the XOR gate that is reliant on the GDI technique. It is composed of four transistors, designated M1, M2, M3, and M4, with input A connected to both gate terminals of transistors M1 and M2. Input B is connected in the same manner to both the M3 and M4 transistor gate terminals. Additionally, input A is connected to the transistor's source M3, and the transistor's source M4 is connected to the drains M1 and M2. To verify the performance logic, the drains of M3 and M4 are linked together.

III. BASIC REVERSIBLE LOGIC GATES

A Reversible Gate is indeed a circuit having k inputs & k outputs (k*k) which always produces the expected result pattern for every possible input pattern[7]. Numerous 3X3 reversible gates have been reported in the literature. Each reversible gate has a cost known as the quantum cost. A reversible gate's quantum cost is the amount of 1 X 1 and 2 X 2 gates or reversible logic gates needed in its construction. For each reversible 1 X 1 and 2 X 2 gate, quantum costs are gathered as a function. This design, also known as the Regulated NOT exit, employs the 1-1 NOT gate and 2-2 reversible gates such as the Controlled-V- and V+ gates, and the Feynman gate[8].

3.1 The NOT Gate

As shown in Figure 4, a NOT gate is also a 1 x 1 gate. Due to the fact that it is a one-to-one gate, its quantum cost would be unity.

Fig.4. CNOT gate

3.2 Feynman Gate(FG):

The Feynman gate is a reversible two-input two-output gate that converts (A, B) to (P , Q), where A, B are the inputs and P, Q are the outputs (FG). Its quantum cost is one. The block diagram of Feynman's gate is shown in figure 5. The Feynman gate can also be used in reversible logic to replicate the signal, thereby avoiding the fan-out issue.

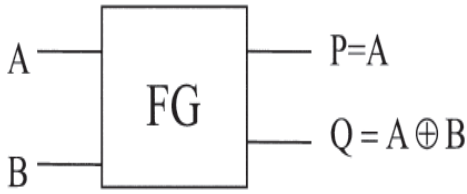Additionally, it would be used to analyze the complement of a signal.

Fig.5 Block Diagram of Feynman Gate

3.3 Toffoli Gate(TG)

As shown in Figure 6, a three-by-three reversible two-through gate is a Toffoli Gate (TG). Two-through guarantees ensuring two of the outputs are identical to the inputs (A, B, C), where the inputs are A, B, C and the outputs are P, Q, R. The Toffoli gate, with a quantum cost of five, is a very popular reversible gate.
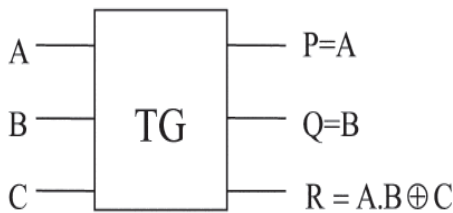

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Fig.6. Block Diagram of Toffoli Gate

3.4 Peres Gate:

A Peres gate is a reversible 3X3 gate that converts (A, B, C) to (P , Q , R), with A, B, C serving as the inputs and P, Q, R serving as the outputs. The Peres gate is shown in Figure 7.
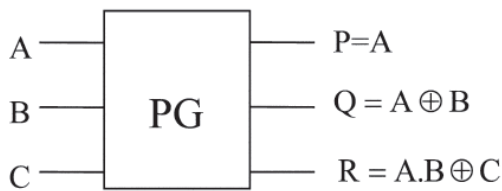

Fig.7. Block Diagram of Peres Gate

3.5 Fredkin Gate

A Fredkin gate is indeed reversible (3X3) gate that converts (A, B, C) to (P, Q, R), where A, B, C are the inputs and P, Q, R are the outputs. It is referred to as a 3x3 gate due to the fact that it may have three inputs & three outputs. The Fredkin gate is shown in Figure 8.
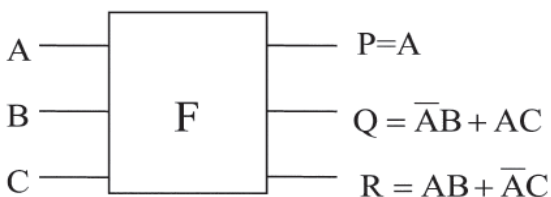

Fig.8. Block Diagram of Fredkin Gate
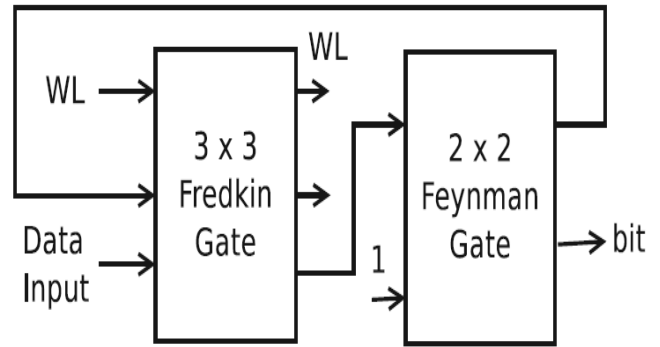
IV. PROPOSED SRAM cell

Fig.9. Proposed Reversible SRAM Cell

This section discusses the write-and-read digital memory cell that is being proposed. The suggested fully reversible system is shown in Figure 9. Because latch & access transistors are immutable, reversible logic is modeled after them. The Fredkin transistors were formerly utilized as control gates. The Fredkin gate's inputs are retained working data, previously stored memory data, and the bit entry. If WL is equal to 0, the third production will be the previously stored data. If WL = 1, the output bit corresponds to the ith input bit. During the reading operation, the SRAM cells are connected to B inputs and B inputs to generate the appropriate output values. To mimic the latch, a single Feynman gate and one Fredkin gate were utilized. The row cells are generated using the WL performance. As a result, the SRAM cell's total life is about 1. If line 2 of Figure 13 is set to 0, the data saved is the output of the three X three Fredkin gate's line 2. The gate is analogous to the input resistor's hold state. If WL = 1, line 2's performance would be utilized. This line 2 is connected to the Feynman circuit through the latch mechanism. By using a 2 X 2 Feynman gate, the single data bit is governed by two 3 X 3 Fredkin gates, and each 2 X 2 Feynman gate controls two of those 3 X 3 Fredkin gates.

The SRAM cell input contains the word line, write, data in, and read signals from the row decoder, and the SRAM cell output contains the write line that is transmitted to the next SRAM cell in the same row, as well as the write line, read line, including data out in the same row. The write signal is the sum of the output side, a Fredkin gate, and trash. If the SRAM cell was read, the bit will be logic 1, otherwise it will be logic 0. The SRAM cell would've been capable of storing whatever value seems to be written to it. When the write signal is zero and the read signal is one, the typical characteristic of the SRAM cell is the value mostly on data output line. The suggested SRAM cell with such a read/write signal costs 16, and when constructed, the trash production is reduced to three.

V. SIMULATION RESULTS

Figure 10 illustrates the simulation results for the SRAM memory. Reversible logic gates have indeed been constructed using the GDI method. SRAM memory is implemented with these reversible gates. The suggested circuit is modelled using CMOS 45nm technology.
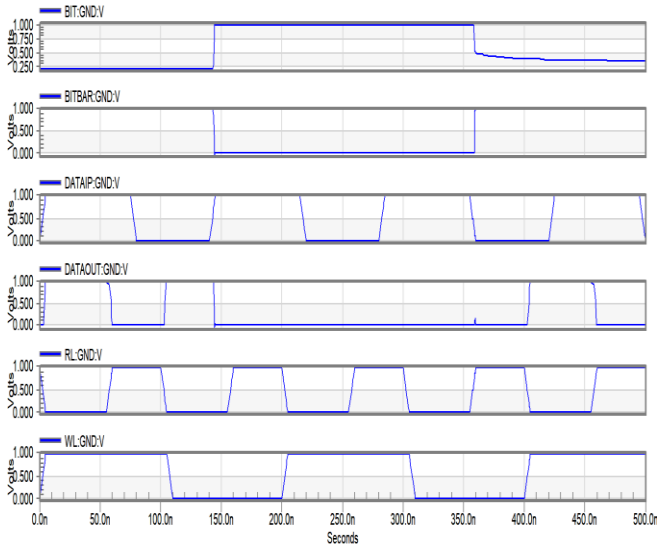
Fig.10. Transient Analysis of GDI technique based reversible logic SRAM

The simulation of the GDI technique-dependent reversible SRAM is shown in Figure 10. The Fredkin gate has three inputs: WL, prior memory data, and the bit entry. If WL equals 0, the third output will be the previously recorded data. If WL equals 1, the third output is the first bit's input. If WL = 0, the data is the output of the three-by-three Fredkin gate. If the value is 1, the resulting value is the input value. This information is sent into the Feynman gate, which is responsible for controlling the latch's mechanism. If the SRAM cell was read, the bit will be logic 1, otherwise it will be logic 0. The SRAM cell would've been capable of storing whatever significance seems to be associated with the data supplied to it. Unless the write signal is '0' as well as the read signal is '1', the SRAM cell value corresponds to the data value.

Table 1: Performance of Different SRAM structures

SRAM type	Constant Inputs	Garbage outputs	Quantum costs	Qunatum Delay	Number of gates	Number of transistors
[9]	3	3	2	19	5	60
[10]	1	1	6	6Δ	2	24
Proposed	2	2	2	2Δ	2	16

From the above table 1, it is evident that the proposed architecture of SRAM is very effective in terms of area delay.

VI. CONCLUSION

We have shown the implementation of several reversible logic circuits using the GDI method. The reversible logic gates have been designed in terms of GDI implementation and then simulated using Tanner EDA Tools. Additionally, the reversible logic gates were used to create the SRAM memory cell. Additionally, we computed and compared many characteristics, including quantum delay and the size of various accessible SRAM cells. As seen in the comparative table, the suggested SRAM design is very efficient in terms of space and quantum delay.

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