Implementation of Full Adder with 18-Transistors using Low Power Design

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***Abstract:** Power consumption has emerged as a primary design constraint for Integrated Circuits (IC's). In the Nanometer Technology regime, leakage power has become a major component of total power. Full Adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU, and the power consumption of an ALU can be lowered by lowering the power Consumption of Full adder. So the full adder designs with low power characteristics are becoming more popular these days. This proposed illustrates the design of the low power less transistor adder designs micro wind tool, the entire simulations have been done on 120nm Single n- well CMOS bulk technology in micro wind tool. This circuit consumes less Power with maximum (18T design) of 84% power saving compare to conventional 30T design.*
***Keywords:** ALU, CMOS, BCD*

I. INTRODUCTION

ADDER: Adders are digital circuits that carry out addition of numbers. Adders are a key component of Arithmetic Logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BCD), Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc.

Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

0	0	1	1
+0	+1	+0	+1
0	1	1	(carry) 1 0

The adder that performs simple binary addition must have two inputs and two outputs. The device which performs above task is called Half Adder.

CMOS TECHNOLOGY:

Complementary metal–oxide– semiconductor (**CMOS**) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal– oxide– semiconductor (or COS-MOS). The words"complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor Material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.**TOOLS USED: IMPLEMENTATION OF CONVENTIONAL DIGITAL FULL ADDER**:
DESIGN :DSCH (DIGITAL SCHEMATIC) LAYOUT DESIGN:MICROWIND
CONVENTIONAL FULL ADDER:

The 1-bit full adder cell has **30 transistors** different logic styles can be investigated from different point of view. The issue of each design is not always attained easily. The conventional full adder consists of 2 EX-R'S,2 AND'S and 1 OR gates.

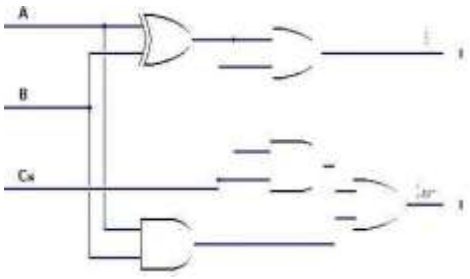

Fig 1 Conventional Full Adder Logic Diagram

The logic is used in the circuits basically effect the speed, area, capacitance and delays and complexity of the circuit. Two important characteristics of CMOS are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. fig.3.1 shows the schematic circuit diagram of full adder (EX-OR,AND,OR) gates using conventional CMOS logic design. This circuit uses the 30-MOS transistors to perform the operation of full adder. In this circuit there is 15 PMOS transistors and 15 NMOS transistors are used.

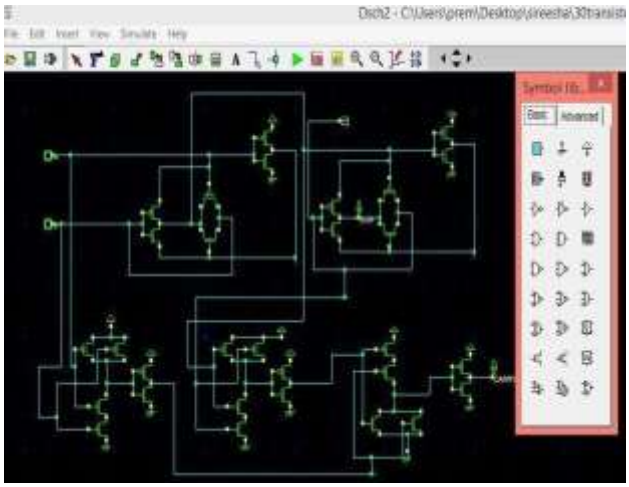

Fig 2. Schematic of Conventional Full Adder

LAYOUT IMPLEMENTATION OF CONVENTIONAL FULL ADDER

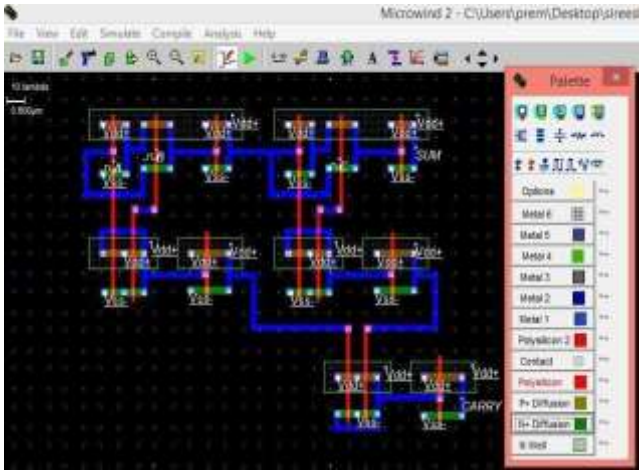

Fig 3. Layout of Conventional Full Adde

II.PROPOSED FULL ADDER:

The full adder circuit can be implemented by various combinations of XOR/XNOR gates and multiplexer blocks. In present approach as shown in block diagram of Fig. 4 (a), we have used two XOR/XNOR cells and transmission gate multiplexer with two transistors to design the full adder. Sum is generated by two XNOR gates as in equation (3) and Cout is generated by two transistor transmission gate multiplexer MUX as in equation (4). Two transistor multiplexers based on pass transistor logic can also be used to generate Count which reduces the total transistor count of adder to 12. Since pass transistor logic shows poor noise margin so in current design transmission gate multiplexer approach has been utilized. For transmission gate multiplexer complementary gate control signals are required and in current design both XOR and XNOR signals are already generated. The single bit full adder using proposed XOR/XNOR cell using 18 transistors has been implemented.

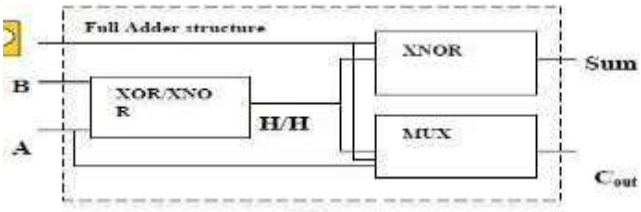

Fig 4.Full Adder Using Xor/Xnor Gates And Multiplexer Block

IMPLEMENTATION OF PROPOSED FULL ADDER

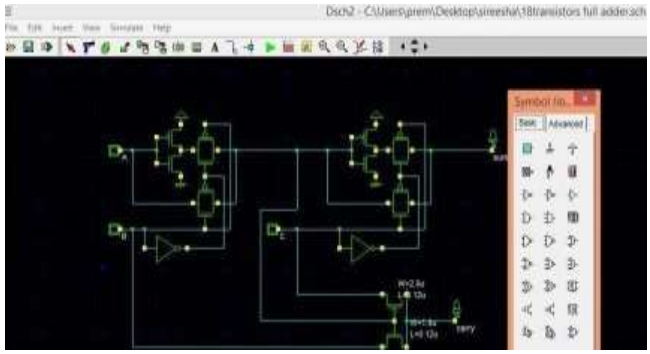

Fig 5. Schematic of Proposed Full Adder

LAYOUT IMPLEMENTATION OF PROPOSED FULL ADDER

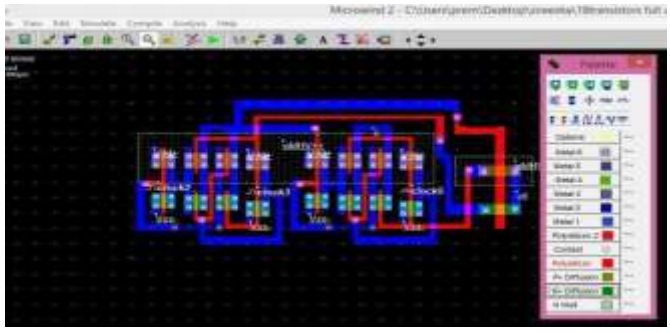

Fig 6.Layout of Proposed Full Adder

III.RESULTS

DSCH SCHEMATIC SIMULATION OF CONVENTIONAL FULL ADDER:

The simulated output waveform of CONVENTIONAL FULL ADDER for voltage vs. time is shown fig. Simulations at the schematic level were performed using DSCH tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential time scale shown in fig

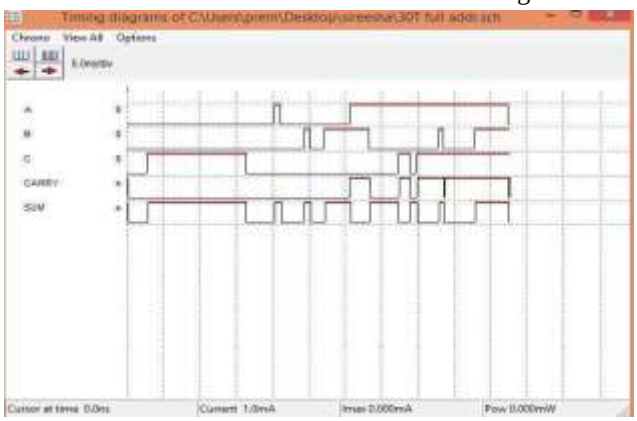

Fig 6.1 DSCH Schematic Simulation of Conventional Full Adder

DSCH SCHEMATIC SIMULATION OF PROPOSED FULL ADDER:

The simulated output waveform of PROPOSED FULL ADDER for voltage vs. time is shown fig. Simulations at the schematic level were performed using DSCH tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential time scale shown in fig.

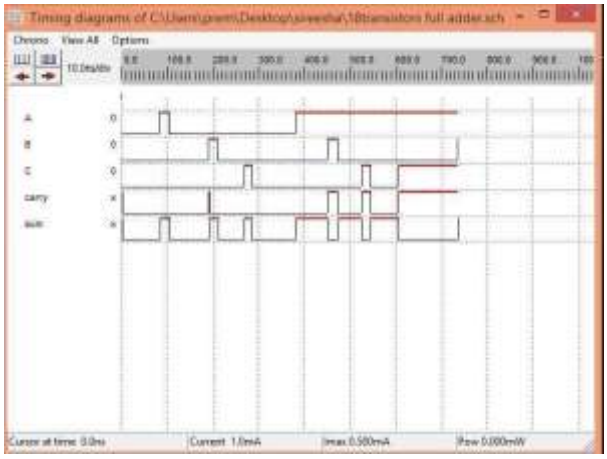

Fig 6.2 DSCH Schematic Simulation of Proposed Full Adder

MICROWIND LAYOUT SIMULATION OF CONVENTIONAL FULL ADDER

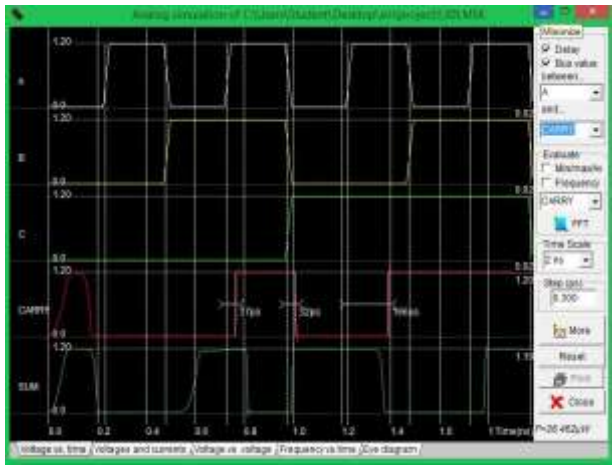

Fig 6.3 Layout Simulation of Conventional Full Adder

MICROWIND LAYOUT SIMULATION OF PROPOSED FULL ADDER

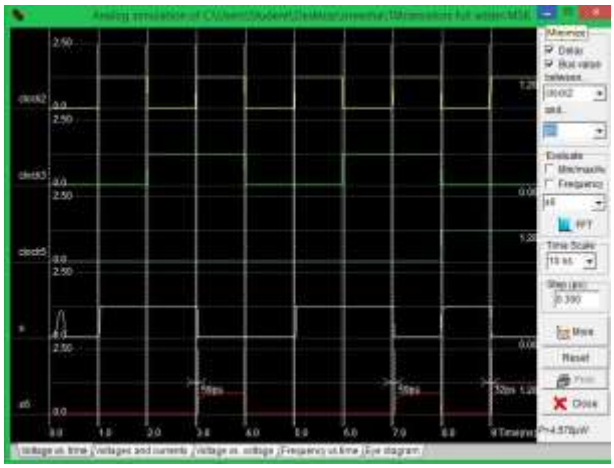

Fig 6.4 Layout Simulation Of Proposed Full adder

COMPARISON OF FULL ADDER PARAMETERS:

FACTOR DESCRIPTION	CONVENTONAL FULL ADDER	PROPOSED FULL ADDER
Number of transistors	30T	18T
Power dissipation	26.462 µW	4.578µ W
Delay	32ps	3ps

IV.CONCLUSION

•The full adder designs have been proposed and simulation results have been compared with the previous results in 120 nm technology using micro wind tool.

•According to the simulation results this circuit consumes less power with maximum (18T) of 80% power saving

compare to conventional 30T design.
Proposed adder also show adequate noise margin with reduced supply voltage.

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