Design of Efficient 32-Bit Parallel Prefix Ladner Fischer Adder

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***ABSTRACT:** A parallel-prefix adder gives the most excellent performance in VLSI design. However, performance of Ladner-Fischer adder through black cell takes large area. So, gray cell can be replaced instead of black cell which gives the Efficiency in Ladner-Fischer Adder. The proposed system hastwo stages of operations they are pre-processing stage and generation stage. The pre-processing stagehaving propagate and generate.Generation stage focuses on carry generation and final result. In ripple carry adder each bit having addition operation is waited for the preceding bit addition operation. In efficient Ladner–Fischer adder, addition operation does not wait for preceding bit addition operation and modification is done at gate level toimprove the speed and decreases the area.*

***INDEX TERMS:** Ripple carry adder, EfficientLadner–Fischer adder,Black cell, Gray cell.*

I INTRODUCTION

Ripple carry adder is used for the addition task i.e., if N-bits addition operation is performed by the full adder with N-bits. In ripple carry adder each full adder operation consists of sum and carry that carry will be given to next bit full adder operation, that processes is continuous till the N^{th} bit operation. The N-1^{th} bit full adder operation carry will be given to the N^{th} bit full adder operation present in the ripple carry adder. [1]

Addition procedure is the main process in digital signal processing and control systems. The high-speed and accuracy of a processor or system depends on the adder performance. Multiplexer is combinational circuit which consists of multiple inputs and a single output. In general purpose processors and DSP processors the addition operation addresses are taken from simple ripple carry adder.

The 3-bit ripple carry adder is shown in Fig.1. The first bit carry is given to second bit full adder and similarly the second bit carry is given to the third bit full adder. The addition process is performed from least significant bit to most significant bit in ripple carry adder[1]. Configuration logic and routing resources in FieldProgrammable Gate Array

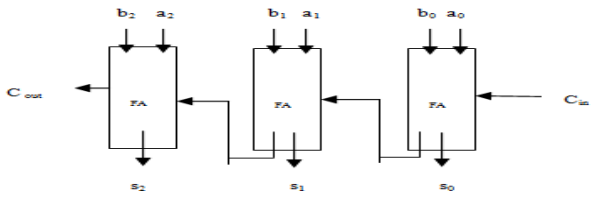

Fig.1: Three Bit Ripple Carry Adder

II LADNER-FISCHER ADDER

Ladner Fischer adder is used for high performance addition operation. The Ladner-Fischer is the parallel prefix adder used to perform the addition operation [3]. It is looking like tree structure to perform the arithmetic operation. The Ladner-Fischer adder consists of black cells and gray cells. [2] Each black cell consists of two AND gates and one OR gate [4]. Each gray cell consists of only one AND gate.p_i denotes propagate and it consists of only one AND gate[5] given in equation 1. g_i denotes generate and it consists of one AND gate and OR gate given in equation 2. [6]

$$p_i = A_i \text{ XOR } B_i \text{ ---------- (1)}$$

$$g_i = A_i \text{ AND } B_i \text{ ---------- (2)}$$

G_i denotes carry generate and it consists of one AND gate and OR gate given in equation 3 used for first black cell. [8]

$$G_i = p_i \text{ OR } [g_i \text{ AND } c_{in}] \text{ --- (3)}$$

III PROPOSED LADNERFISCHER ADDER

The proposed Ladner-Fischer adder is flexible to speed up the binary addition and the arrangementlooks like tree structure for the high performance of arithmetic operations.

Field programmable gate arrays [FPGA's] are mostly used in recent years because they improve the speed of microprocessor based applications like mobile communication, DSP and telecommunication. Research on binary operation fundamentals and motivation gives development of devices. The construction of efficient Ladner-Fischer adder consists oftwo stages. They are pre-

processing stage and generation stage.

Pre-Processing Stage:

In the pre-processing stage, generate and propagate are from each pair of the inputs. The propagate gives "XOR" operation of input bits and generates gives "AND" operation of input bits [7]. The propagate (P_i) and generate (G_i) are shown in below equations 4 & 5.

$$P_i=A_i \text{ XOR } B_i \text{ ------ (4)}$$

$$G_i=A_i \text{ AND } B_i \text{ ------ (5)}$$

Generation Stage:

In this stage, carry is generated for each bit is called carry generate (C_g) and carry is propagate for each bit is called carry generate (C_p). The carry propagate and carry generate is generated for the further operation, final cell present in the each bit operate gives carry. The last bit carry will help to sum of the next bit simultaneously till the last bit. The carry generate and carry propagate are given in below equations 6 & 7.

$$C_p=P_1 \text{ AND } P_0 \text{ ---------- (6)}$$

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ (7)}$$

The above carry propagate C_p and carry generation C_g in equations 6&7 is black cell and the below shown carry generation in equation 8 is cell i.e., gray cell. The carry propagate is generated for the further operation. The final cell present in the each bit operation gives carry. The last bit carry will lead to sum of the next bit simultaneously till the last bit. This carry is used for the next bit sum operate, the carry generate isgiven in below equations 8.

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ (8)}$$

The carry of a first bit is XORed with the next bit of propagates then the output is given as sum and it is shown in equation 9.

$$S_i=P_i \text{ XOR } C_{i-1} \text{ ------- (9)}$$

It is used for two thirty-two bit addition operations and each bit undergoes pre-processing stage and generation stage then gives the final sum.

The first input bits goes under pre-processing stage and they will produce propagate and generate. These propagates and generates undergoes generation stage produces carry generates and carry propagates then gives final sum. The step by step process of efficient Ladner-Fischer adderis shown in Fig.2.

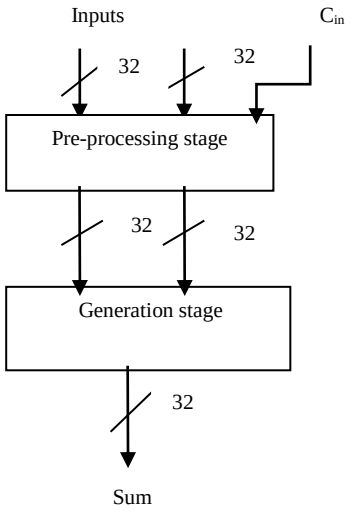

Fig.2: Block Diagram

The efficient Ladner-Fischer adder arrangement is looking like tree structure for the high performance of arithmetic operations and it is the high speed adder which focuses on gate level logic. It designs with a reduction of number of gates. So, it decreases the delay and memory used in this architecture.

The efficient Ladner-Fischer adder is shown in fig.3 which improves the speed and decrease the area for the operation of 16-bit addition. The input bits A_i and B_i concentrates on generate and propagate by XOR and AND operations respectively. The propagates and generates undergoes the operations of black cell and gray cell and gives the carry C_i. That carry is XORed with the propagate of next bit, that gives sum.

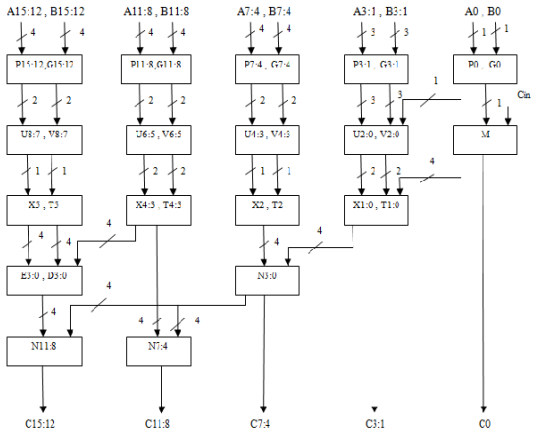

Fig.3: 16-Bit Efficient Ladner-Fischer Adder

The properties of the operations are evaluated in parallel with accept the trees to overlap which leads to parallelization. The architecture of Efficient Ladner-Fischer adder gives the less delay and less memory for the operation of 16-bit addition.

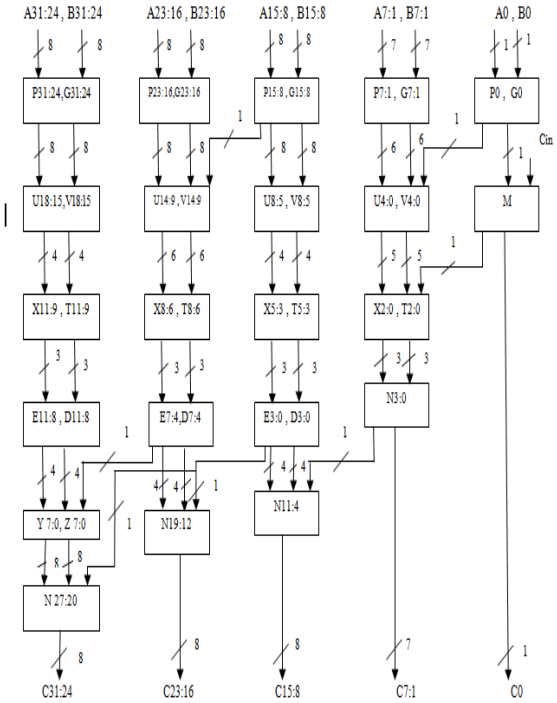

Fig.4: 32-bit Efficient Ladner-Fischer Adder

The architecture of 32-bit Efficient Ladner-Fischer adder is shown in Fig.4. The logical circuit is using multiple adders to find the output i.e., sum of N-bit numbers. Each addition operation has a carry input (C_{in}) which is the previous bit carry output (C_{out}).

Research on binary addition innovatively motivates gives development of devices. Many parallel prefix networks describe the literature of parallel addition operation.The parallel prefix adders are Ladner-Fischer, Kogge-stone, Ladner-Fischer, Sklansky, etc,. The fast and accurate performance of an adder gives to used in the very large scale integrated circuits design and digital signal processors.

IV SIMULATION RESULTS

The Efficient Ladner-Fischer adder is design with an VHDL (very high speed integration hardware description language). Xilinx project navigator 14.1 is used andSimulation results of 32-bit efficient Ladner-Fischer are shown in Fig.5.

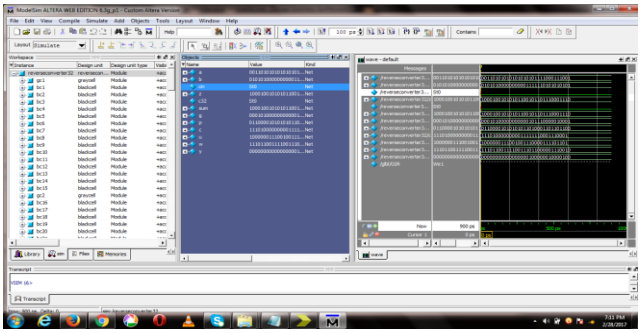

Fig.5: 32-Bit Efficient Ladner-Fischer Adder Simulation Waveform

The design of adders is done on VHDL. The memory and delay performance Efficient Ladner-Fischer adder (ELF) is shown in Table.1

Adder	Delay(ns)	LUT's Used
16-bit Ladner-Fischer adder	43.092	63
32-bit Efficient Ladner-Fischer adder	30.330	93

Table.1: Delay and memory used in ELF

V CONCLUSION

In this paper, new approaches to design an efficient Ladner-Fischer adder look like tree structure and cells in the carry generation stage are decreased to speed up the binary addition. It concentrates on gate levels to perk upthe speed and decreases the memory used.The proposed adder addition operation offers elude great advantage in reducing delay.

REFERENCES

[1] Pakkiraiah chakali, madhu kumar patnala "DesignOfhigh speed Ladner - Fischer based carryselectadder" IJSCE march 2013
[2] David h,k hoe, Chris Martinez and sri jyothsna vundavalli "Design and characterization ofparallel prefix adders using FPGAs", Pages.168-172, march2011 IEEE.
[3] K.Vitoroulis and A.J. Al-Khalili, "performance of parallel prefix adders implemented with FPGA technology," IEEE Northeast Workshop on circuits and systems, pp.498-501, Aug. 2007.
[4] Haridimos t.vergos, Member, IEEE and Giorgos Dimitrakopoulos, Member, IEEE,"On modulo2^n+1 adder design"IEEE Trans on computers, vol.61, no.2, feb 2012
[5] GiorgosDimitrakopoulos and DimitrisNikolos, "High-Speed Parallel-Prefix VLSI Ling Adders"IEEE Trans on computers,

vol.54, no.2, Feb. 2005.

[6] S.Knowles,"Afamily ofadders," Proc.15th Symp. Comp. Arith.,pp.277-281,June2001.

[7] R.LadnerandH.Fischer,"Aregular layout for parallel adders,"IEEETrans.Computers,vol.C-31,no.3, pp. 260-264,March1982.

[8] R.E. Ladner and M.J. Fischer, "Parallel Prefix Computation," J. ACM, vol. 27, no. 4, pages 831- 838, Oct. 1980.