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# Structural Changes to Improve MOSFET Performance And Introduction of New Materials: A Review

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Abstract: Silicon dioxide interface permits excellent metal-oxide-semiconductor field-effect transistors (MOSFETs) to be fabricated. These devices have many properties, like operation frequency and power consumption that improve as their size is scaled right down to smaller dimensions that additionally permit additional transistors to be packed onto a chip. The smaller sizes are achieved mistreatment higher-resolution lithography that is improved by steady up the fabrication technologies. The trends of steady rising performance and larger integration density with time are generically cited as "Moore's Law". Of course, scaling should finish eventually, somewhere before the size of atoms is reached. So as to fulfill the requirement for low off current whereas keeping power consumption in restraint, the semiconductor trade is functioning to introduce high-k gate dielectrics in multi gate semiconductor device producing method. The fundamental device parameters for various dielectric materials within the MOSFET, Gate designed MOSFET and channel designed MOSFET devices are mentioned in this paper.

Keywords: FinFET, High-k dielectric, Gate stack, Short channel effects (SCES), Equivalent oxide thickness (EOT)

#### **I.INTRODUCTION TO MOSFET**

### i. New Materials

Materials like Ge will offer larger carrier densities, however the low bandgap may be a extended disadvantage unless quantum confinement will be wont to increase the bandgap in structures of sensible dimensions. High-k dielectrics square measure designed. To address one specific aspect of off-state power consumptions: tunneling currents. It's probably that gate the gate dielectric thickness is going be the to primary parameter to achieve atomic dimensions. This can be as a result of the dielectric thickness indirectly controls the gate length. In general, the effective gate length needs to be forty times the dielectric thickness to properly control short channel effects (SCE). Thus, the that reduces scaling gate length should conjointly reduce the dielectric thickness. However, because the dielectric thickness decreases, electron tunneling through the dielectric becomes a major issue. The planned answer to the current downside is to seek out a cloth that includes a higher k worth than the SiO2 used at the moment because the gate dielectric. This is to permit the actual thickness able of the be enlarged whereas gate dielectric to still maintaining a similar electric field within the channel. Whereas this sounds sensible in theory. implementation has proven to be difficult. To do this, a material should be found that meets several criteria. The material should be

compatible with the encircling Si and also the fabrication processes used. Also, it should have a breakdown time a minimum of as long as silicon oxide. Whereas there are several different necessities, serve it to mention that several materials are proposed, however no smart substitute has vet been found. ii. New Structures

# Nano Size High-K Dielectric

Now a day, the globe is turning into smaller by the Moore's law states that the scale of the transistors compressed to double the would be amount of transistors in every eighteen months. The 2010 ITRS (International Technology Roadmap for Semiconductor) update clearly explained that we have tendency to are progressing towards higha k dielectric materials which will replace the SiO2 within the MOSFET. Thus here we've created an endeavor to seek out the choice dielectric material for MOSFET.Indeed, the

traditional gate dielectric SiO2 clearly cannot survive challenge the of an EOT (Effective oxide Thickness)= 1 nm. So it is extremely desirable that materials with high dielectric constants and lesser physical thicknesses are going to be used for MOSFET devices. A figure of merit to gauge a gate oxide high-k dielectric material laver is that the equivalent oxide thickness (EOT). The EOT shows the effective oxide thickness of the highk dielectric material layer SiO2 when the to

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capacitance is that the same. Since a thicker layer is employed for insulating, the tunneling current is drastically reduced during this thickness regime.



Fig.1 High-k gate dielectrics for further scaling However, before a brand new high-k material is integrated into the current ULSI (Ultra large scale

integration) method flow, several needs have to be compelled to be met first. However, as technology evolves, SiO2 can shortly reach its physical limitation like high off current and reliableness considerations (ITRS

2010). Continuing scaling down of the MOSFET device with the minimum feature size of 90 nm and below would need thinner EOT. In this thinner EOT range, SiO2 suffers from high off current and is incredibly troublesome for low power applications. Therefore the next various highk dielectric materials for future CMOS technology is proposed.

### **II. Requirements for high-k gate dielectrics**

Selection of high-k materials is incredibly vital. in the past years, several firms, universities and research organizations spent efforts investigation a large vary of high-k materials candidates for continue scaling of MOSFET. The most criteria for choosing high-k materials manufacturability, integration were capabilities. and semiconductor unit performance. some necessities for choice of high-k There are materials, like high dielectric constant, wide band gap, conduction/valence band offsets with Si substrates, thermal stability, nice electrical interfaces. amorphous part and direct contact with Si substrate Figure 2 shows the connection of static dielectric constant and band gap for candidate gate oxide, wherever one will observe a decreasing trend in bandgap with higher dielectric constant. There are plenty of materials are researched to accommodate new gate insulator for MOSFET, particularly metal oxide like Al2O3, ZrO3, HfO2 and lanthanide oxides are expected to be the gate insulator for next generation.



Figure 2: Bandgap of different High-k materials **i. Aluminum Oxide (Al2O3)** 

Aluminum oxide (Al2O3) has the potential to be used for future generation devices due to its special physical and chemical properties. Al2O3 has a large band gap of about 8.8 eV. It has thermal stability as well as highbarrier offset in nature. Al2O3 is also an alternative for conventional gate dielectric material because of its high crystallization temperature, so it is compatible with conventional process of integrating complementary MOS devices, which involves high temperatures above 1000°C. Al2O3 exhibits gate leakage much lower than that of conventional SiO2 of effective oxide thickness (capacitance) and also provides good interface quality. But the drawback of Al2O3 is that it has bad waferleakage uniformity compared to Zirconium-di-oxide.

# i. Aluminum Oxide (Al2O3)

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with typical method of integrating complementary MOS devices, which involves high temperatures on top of 1000°C. Al2O3 exhibits gate leakage abundant less than that of conventional SiO2 of effective oxide thickness (capacitance) and additionally provides smart interface

quality. However the downside of Al2O3 is that it's unhealthy wafer-leakage uniformity compared to Zirconium-di-oxide.

### ii. lanthanum oxide (La2O3)

La-silicate gate dielectrics is that an instantaneous contact of high-k/Si structure is simply achieved by merely depositing La2O3 on Si substrate attributable to the reactively formation of La-silicate by the reaction between La2O3 and Si

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throughout hardening method, dielectric constant of La-silicate dependent to provide of oxygen atoms, excess provide of oxygen atom increase dielectric constant because of formation of Sirich La-silicate.

# iii.Titanium-Di-Oxide (TiO2)

TiO<sub>2</sub> is taken into account because the alternative gate dielectric for SiO2. Even if the electronic band of this material is gap comparatively little (3.5 eV). its dielectric constant may be varied from 40 to 110. Reckoning growth method, on the TiO2 presents two vital phases, Anatase and Retile. The last part is that the thermally stable part that presents the higher dielectric constant, just about 80; Anatase may be a thermally unstable part with lower dielectric constant reworking in Retile part at temperatures over  $600^{\circ}$ . Although TiO2 includes a terribly high dielectric constant, its unhealthy thermo dynamic stability with Si and enormous band gap thus it's not most well-liked in devices.

### iv. Hafnium-Di-Oxide (HfO2)

HfO2 are often thought-about because the most promising stuff chemical compound material to interchange SiO2 gate stuff as result а of it's thermodynamically a lot of stable on Si than the other high-k materials. HfO2 devices have incontestable several orders of magnitude reduction in gate leak with associate degree EOT of around one.0 nm for innovative transistors. HfO2 shows superior properties as a result of its higher highk material worth and less degradation for ultrathin films. Though the band gap of HfO2 is smaller than Al2O3, each physical phenomenon Band Offset and Band Offset are already Valence larger than two electron volt for HfO2 with reference to Ge. And conjointly the Nano size material synthesis is troublesome in HfO2.

# v. Zirconium as High-k Materials

Zirconium is that the most applicable metal chemical compound since it's thermodynamically stable with SiO2. Thermally Stable high-k stuff material is principally ZrO2, since it's a stuff worth of twenty five, an oversized energy band gap, (5.16 eV to 7.8 eV). The nano size particle is often synthesized for ZrO2 in MOS fabrication, considering the actual fact that the nano sized ZrO2 is that the best alternate for SiO2 in future MOS technology.

To control short-channel effects, the influence of the

gate voltage on the channel electrons arising within interface should be inflated. to the MOS the present purpose, it's effective to form the channel especially skinny film (thin-film laver an body structure) as in thin-film Si-On-Insulator (SOI) devices and, further, to create the gate electrodes around this (multi-gate structure). due thin-film body to the above, we can we are able to assume that the channel structures will progress so as from single gate FETs on thin-film SOI to double gated dual-fin-FETs, triple gated tri-gate FinFETs and eventually nanowire FETs within which the gate electrode is wrapped round the channel sort of a wire, as is shown schematically in Figure 3. very recently, Intel Corporation created it clear that FinFETs would be utilized inMOSFETs for the 22 nm technology node, and that we have come back to the age when thin-film body structured multigate structures can finally be achieved. With this device structure, the short-channel effects are often controlled, not by the electrical field shaped by substrate impurities, however by the consequences of the shape of the physical structure.



Figure3: Structural changes of MOSFET An intrinsic channel that contains no impurities will be used for the channel, and therefore the variations in threshold value and variations in characteristics attributable variations to the in impurities will be reduced by controlling the threshold value exploitation the gate electrode. On the there are issues with other hand, the extremely precise process technology for forming three-dimensional MOSFET structures, reducing parasitic resistance and capacitance and achieving MOSFETs with completely different threshold values

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on the same substrate. **IV.CONCLUSION** 

The decrease of device dimensions has semiconductor diode to the requirement for different, high material constant (k) oxides to switch silicon oxide as the gate dielectric in complementary metal oxide semiconductor (CMOS) devices. Increase of standard CMOS performances implies a reduction of transistors dimensions. Keeping a high drain current level with a reduced gate length may be achieved by reducing the gate equivalent compound thickness (EOT). Metal gate electrodes needed for nanoscale bulk electronic transistors and advanced transistor structures.

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