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Design of high gain Low Power Operational Amplifier

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Abstract— In this paper we are going to design a two stage CMOS operational amplifier and to analyses its behavior by performing AC analysis using tsmc 130nm technology of mentor graphics tool. Generally Op-Amp is an electronic device that produces high gain which is required in almost all the applications. All the analog circuit fabrication processes are using Op-Amp as the basic component. Thus it is essential to make sure that op-amp must operate very effectively. So we try to increase the gain of op-amp by using two stages with CMOS realization. Here CMOS is used since it provides less power dissipation and requires only 5V as input for biasing. We are modifying the existed design by placing a current source in place of biasing circuit and operating all the components in saturation region only. Thus, we are accomplishing the function of biasing circuit with a current mirror circuit. Also, the area used to fabricate the circuit is also less as we are reducing the number of MOS transistors used to design the circuit. Hence this two stage Op-Amp produces high Gain, Phase Margin. The simulation results are provided by using mentor graphics tool showing the graphs of gain, phase margin and the slew rate.

Index Terms—Mentor Graphics Tool, CMOS realization, 130nm technology, Current mirror circuit, Gain, Phase margin.

I.INTRODUCTION

The industry of electronics has exploded over past years. MOS markets have dominated large amount of worldwide sales. In Mean time CMOS technology succeeded to attain very small feature sizes. Designing of analog integrated circuits with high performance are having more demand because of persistent trend in direction of reduced voltage supplies and transistor channel length. The higher performance of MOS transistor is because of fact that smaller dimensions can be achieved by scaling. Now-a-days we are trying to make the transistor size as small as possible, even up to nanometer ranges.

In many electronics systems the main building block is Operational Amplifier. Generally an Op-Amp which is direct coupled amplifier having high gain composed of differential amplifiers, level translator and a push-pull or complementary-symmetry pair as the final output stage. An Op-Amp is used for the amplification of both ac and dc signals. Presently it is using for different applications like active filters, oscillators, comparators, and others.

The Op-Amp design tends to create challenges as scaling factor for supply voltage and for the channel length of transistor reduces with generation of different CMOS technologies. The tradeoff among different parameters like power, gain, speed will be there at several ranges of the aspect ratio. Here the problem is to realize the CMOS Op-Amp that shows desirable dc gain with unity frequency gain. To overcome this problem we are having several circuit approaches.

The main aim is to design a high gain two stage CMOS Op-Amp by proposing a straight forward design methodology with accurate equations. It is done by performing analysis with the parameters like gain, phase angle, bandwidth etc. This design methodology can be applicable to various amplifier architectures. The results of simulation are obtained by using the tsmc 130 nanometer CMOS technology. Mentor Graphics tool was used to carry out the design. Model Sim Eldo and Design Architect IC are used to verify the simulation results.

Blocks of two stage cmos op-amp

In analog circuit designing the basic component is an operational amplifier. DC gain and Bandwidth of Op-Amp gives the accuracy and speed of the analog circuits. As the bandwidth and gain are large the speed of the Op-Amp is also high.

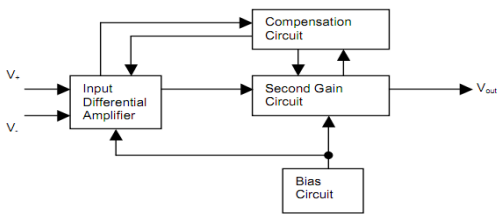

Fig.1 Basic blocks of an Op-Amp

The figure shows the different stages that constitutes an Op-Amp. Inputs, namely inverting and non inverting input voltages, are given to initial stage of Op-Amp called Input Differential Amplifier. The difference between inputs values is obtained as output from differential amplifier as voltage or current based on requirement. There is an intermediate stage in between differential amplifier stage and second gain circuit stage used to get single ended output function called single-ended converter stage. This stage is not required in some type of architectures and so this stage is ignored.

In almost all the circuits the gain obtained by input stages is never upto requirement so in such cases additional amplification must be provided. For this purpose we use one more differential amplifier with output of first stage as inputs. In This stage the additional gain is provided as it uses differential input unbalanced output differential amplifier. Next block is bias circuit, used to provide each transistor with suitable operating point to operate in saturation regions. Compensation circuit, is the another important block used at the high frequencies to lower gain and attain stability when we apply negative feedback to the Op-Amp. Finally the output stage used to have large output currents and the low output impedance or for betterment of slew rate. In case Op-Amp is used to drive purely small capacitor load in applications like data conversions there is no need to use the Output buffer and such circuits in which output buffer stage is not essential and is eliminated are known as the operational transconductance amplifier, OTA. Thus all these blocks constitute the basic Op-Amp.

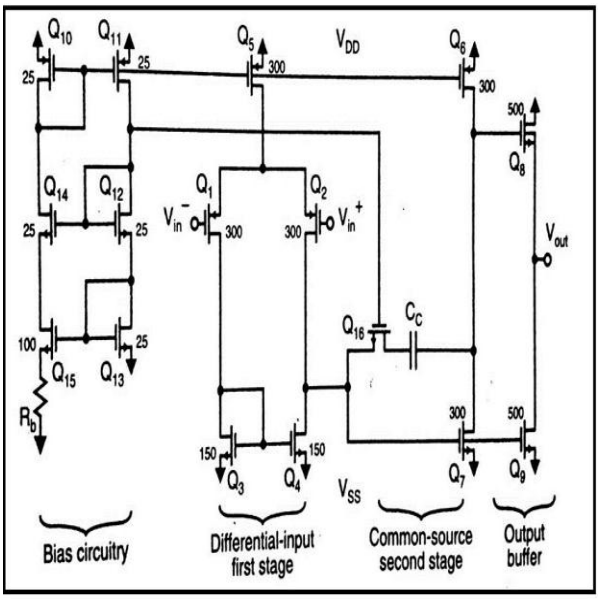

Fig.2 CMOS realization of 2stage Op-Amp

The CMOS realization of Op-Amp is as shown in Fig.2. It resembles the circuit implementation of each block shown in block diagram of Op-Amp. The design used in this realization faces problem in obtaining required amount of gain and thus the slew rate.

The each block in basic Op-Amp shown in fig.1 is replaced with an actual circuit implemented in VLSI technology. All the stages like differential amplifier, second gain stage, bias circuit, output buffer stages are shown in the figure.

To overcome the problems in the present CMOS realization of Op-Amp like low gain value and low phase margin we move to the new design methodology to have the high gain and slew rate.

II. OPERATION OF CIRCUIT

The design of final circuitry must satisfy the desired specifications and design is as shown in the Fig.3. The circuit topology is as standard CMOS Op-Amp. This topology successfully satisfied all design specification by comprising of basic subsections like differential gain stage, bias strings and second gain stage.

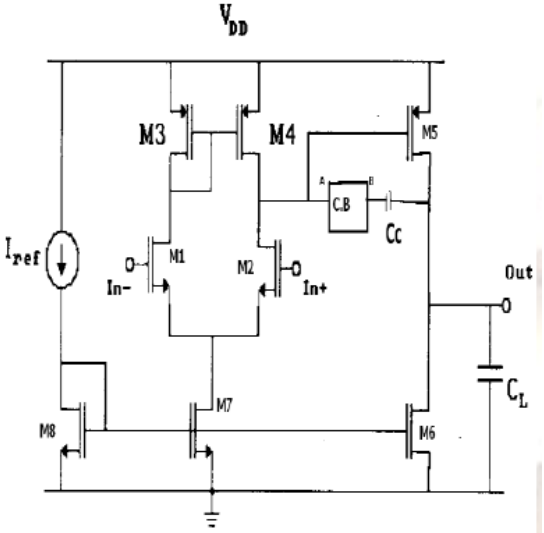

Fig.3 Topology for design of Op-Amp

III. DIFFERENTIAL INPUT STAGE

The initial stage of the Op-Amp comprises of differential amplifier with a single ended converter represented by transistors namely M1, M2, M3 and M4. Among these M1, M2 transistors are N channel MOSFETs forming input differential amplifier stage. The inverting input and non inverting input are given to transistors M1 and M2 respectively. The differential input signal applied to input terminals is amplified as per

gain of the differential stage. The gain of first stage is equal to the transconductance of M2 times the total output resistance at drain of M2. The output resistance is mainly due to M1, M2 and active loads of M3, M4. For performing single ended conversion we use current mirror circuit with transistors M3 and M4. In this the use of current mirror load helps to have large output resistance and
helps with CMRR. The current from M1 is mirrored by M3, M4 and is been subtracted from M2 current. The output resistance gets multiplied with the differential current from M1, M2 giving out single ended output to use as input to second stage.

Second stage for additional gain

The current sink load inverter represents second gain stage It is known that second stage is used to provide additional gain, here transistors M5 and M6 used for that purpose. The M5 transistor, is in common source configuration amplifies the output taken from drain of transistor M2. The M6 transistor is an active device used as load resistance for M5. The gain obtained is equal to transconductance of M5 times the effective load resistance results from M5, M6 output resistances. The M7 is used as load where as M6 acts as a driver.

Bias string

For providing the proper biasing to the Op-Amp we use four transistors. A current mirror bias string is formed with transistors M8 and M9 for supplying a voltage to gate and source of M7 and M6.In order to make sure that M8 and M9 transistors operate in the saturation region they are diode connected. For the remaining transistors biasing is controlled by node voltages. Transistor M5 is biased by gate to source voltage(VGS) provided by VGS of current mirror load.

design of op-amp

The main aspect to be taken into account while designing a circuit is to meet the required specifications.

NAME OF SPECIFICATION	NUMERICAL VALUES
Supply Voltage (VDD)	5V
Required Gain	>70db
Settling Time	1u Sec
Gain Bandwidth	10MHz
Offset value	1-2v
Slew Rate	10 V/uSec

Table. 1 Custom Design Specifications Of Op-Amp

Design methodology of op-amp

The necessary relations are as follows:

$g_{m1} = g_{m2} = g_{mI}$, $g_{m5} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$

$$Id = \frac{\mu_{n,p}\, Cox \left(\frac{W}{L}\right) Veff\, 2}{2}$$

$$g_m = \sqrt{2\mu_{n,p} Cox \frac{W}{L} Id}$$

$$g_m = 2\frac{Id}{V_{eff}}$$

$$\text{Slew rate} \quad SR = \frac{I_5}{C_C}$$

$$\text{First stage gain } A_{v1} = \frac{-gm_1}{gds_2 + gds_4} = \frac{-2gm_1}{I_5\,(\lambda_2 + \lambda_4)}$$

$$\text{Second stage gain } A_{v2} = \frac{-gm_6}{gds_6 + gds_7}$$

$$\text{Gain Bandwidth} \quad GB = \frac{gm_1}{C_C}$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$$

All the transistors (M1-M9) are assumed to be operated in saturation region for calculating the above mentioned relations.

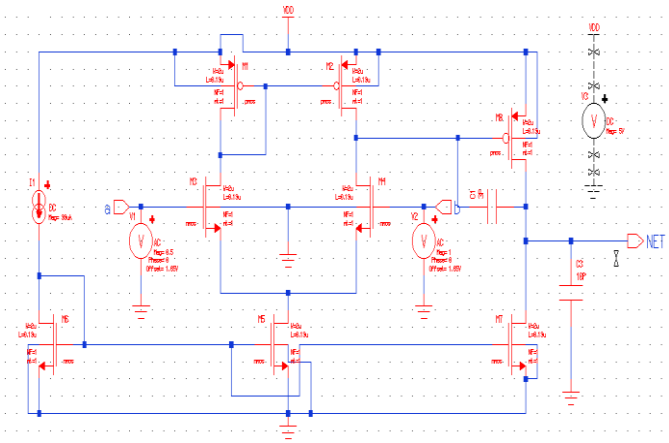

Fig.4 Schematic of two stage CMOS Op-Amp design

This paper deals with designing of two stage Op-Amp with input given to n- channel pair. In order to make the ac signals move above and below the ground, dual polarity is given to Op-Amp and is also centered at ground. Using the Model Sim Eldo of Mentor Graphics the circuit analysis is made and the schematic is as shown in Fig.3

Open loop gain: It is the ratio between maximum output voltage and the differential input voltage is known as open loop gain.

Slew Rate: The change in output voltage per change in the unit time dVo/dt is termed as slew rate. The output signal slope represents slew rate.

Rise time : Time attained by output to reach the final value from 10% to 90% is called as rise time.

CMMR: The ratio between common mode gain and differential gain is known as Common Mode Rejection Ratio.

IV. SIMULATION RESUTS

To analyze how the basic two stage CMOS Op-amp design behaves we perform ac analysis. Let us see the results:

AC ANALYSIS:

In the AC Analysis, calculate the Phase Margin, Gain in db of Op-amp.

- With Start Frequency = 1HZ.
- With Stop Frequency = 10KHZ.

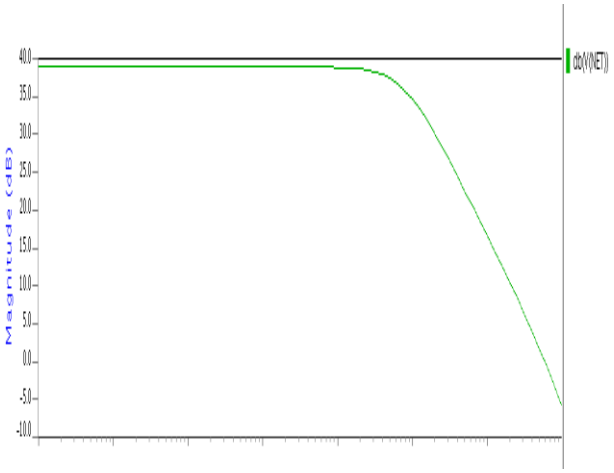

Fig.5 Magnitude of Op-amp in AC analysis

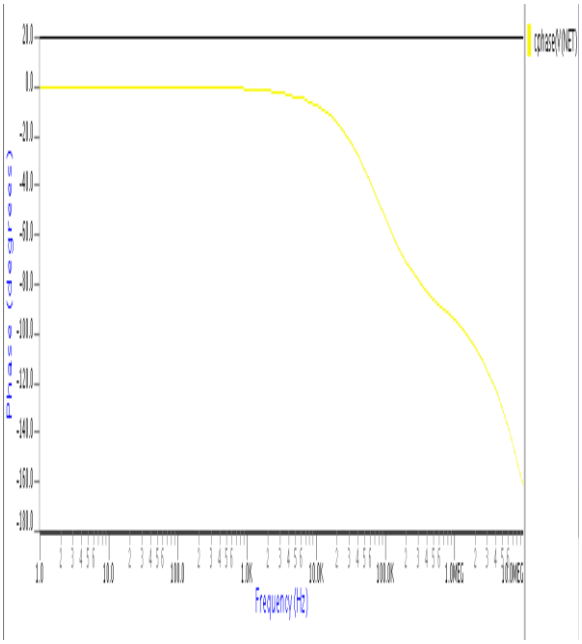

Fig.6 Output phase of Op-amp in AC analysis

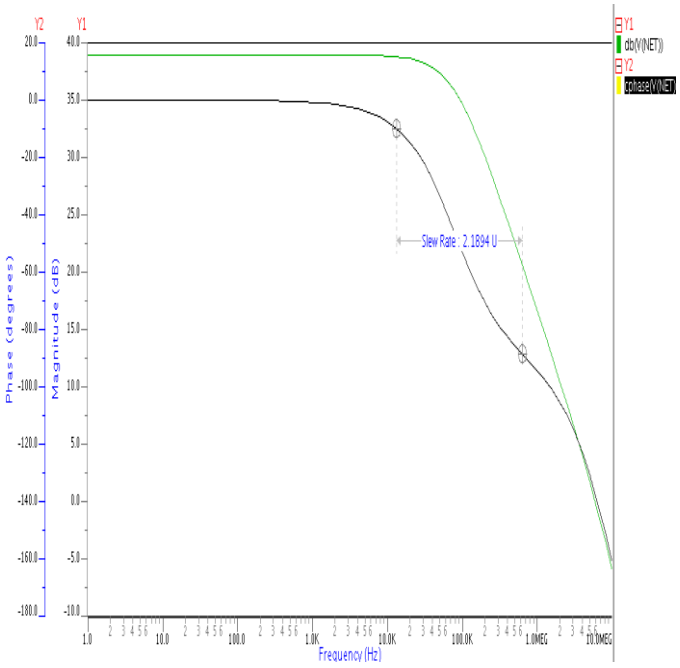

Fig.7 Result of slew Rate

With this design, slew rate obtained is 2.38 V/uSec.

V. CONCLUSION

The two stage Op-amp with CMOS implementation and the analysis of Op-amp behavior is presented in this paper. The results of the design technique, corresponding calculations and the computer aided simulation are presented in detail. The gain obtained with this presented design is high compared to basic circuit. The Result shows that the designed Op-amp satisfies the specifications.

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