FULL ADDER USING CMOS TECHNOLOGY

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Abstract*: In this Paper, a CMOS Full Adder is designed using Tanner EDA Tool based on 0.25µm CMOS Technology. Using Tanner software tools, schematic and layout simulations as well as the schematic versus layout comparisons of CMOS full adder are designed and presented, which helps to obtain accurate design constraints. As part of this we have performed the simulation of CMOS full adder using T-SPICE and BSIM3v31 tools of Tanner EDA. The parameters of power consumption, Area, Propagation Delay, and Power Delay Product (PDP) are evaluated to analyze the proposed one-bit full adder

I. INTRODUCTION

Complementary metal-oxide semiconductor (CMOS) logic is used in integrated circuit, microprocessors, microcontrollers and other digital logic circuits for to reduce power consumption and being more immune towards noise occurring conditions. In the CMOS there are complementary and Symmetrical pairs which are of P-type (PMOS) and N-Type (NMOS) which are used for implementation of logic functions. In a PMOS transistor we can have input from voltage source or from other PMOS transistor. NMOS transistor can have input from ground or other NMOS transistor. Low power, high noise margin, design ease, functionality are the main advantages of CMOS and high input capacitance reduces the ultimate performance are the disadvantages.

Table 1: Parameters of PMOS and NMOS

Parameters	PMOS	NMOS
Low resistance	Low gate voltage	High gate voltage
High resistance	High gate voltage	Low gate voltage

II. FULL ADDER

Full adder adds the incoming inputs and gives the result along with a carry. From a figure (1) a 1-bit full adder takes three inputs and gives two outputs which are sum and carry. A full adder contains two half adders which are being connected to input A and B of one half adder and other is being connected to sum (output)which have the one input as C_{in} and other is the output of XNOR table(2). The arithmetic operations in multipliers, compressors, large adders, comparators and parity checks are done by full adder which is the fundamental unit in the above circuits, which also reduces the power consumption [3].

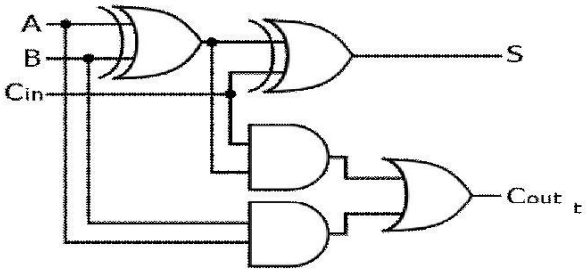


Figure1.Logic diagram Full Adder

Table 2: For Full Adder:

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. CONVECTIONAL FULL ADDER

Convectional full adder is a typical full adder which has more number of transistors like 28T and minimum of transistors like 11T [1]. Here in this paper I have implemented a 28 transistor convectional full adder. It is similar to full adder but the main difference is that the number of transistors we use here increases.

IV. HALF ADDER

Half adder is the basic building block of all

arithmetic circuits. Half adders are present on every microchip or any machine to perform addition, subtraction, division and multiplication [2]. To any half adder we give two binary inputs, namely A and B and two outputs namely sum and carry. Depending on the transistors, the performance of half and full adders change accordingly. If low number of transistors are used the noise and area reduces. Similarly, If more number of transistors are used the noise and area increases. In this paper a one bit full adder is being proposed using CMOS technology which is being implemented using Tanner tool. There are many technology values existed but here technology 2.5v is used for this implementation.

In this paper the power dissipation and propagation delay are measured. The product of these values gives get the power delay product, which shows the resistance value it, is having.

$$P_d=(I_d*V_{dd})+(C_L*F*V_{dd}^2)$$

V. TANNER TOOL

Tanner EDA tool is for analog and digital signals integrated circuits and its design offers efficient path from design captured through verification. In this we can use different applications including power management, Display image sensors, Bio-medical, Automotive and consumer electronics. In this tanner we have several specialty tools to enhance our productivity depending upon our requirement .Different specialty tools are layer fill, Pad IO Cross-Reference Extractor (Pad Map), Wafer tools and Node Highlighting. In tanner micro electrical mechanical systems (MEMS) designs have been tapped out. Mechanical Design Tools can perform few No Boolean Operations, have no Design Rule Checking, limited scripting capability, and limited hierarchical structure so operations are slow in performing and simple layer render makes it difficult to view overlapping geometries. Compared to mechanical design tools tanner can perform enhanced Boolean operations, perform design rule checking (DRC), in this hierarchical structure makes operations fast and is easy to review overlapping Geometries [6].

VI. DESIGN ASPECTS

In this paper I am using the tanner tool to implement the convectional full adder having 28 transistors in number [4]. The process of making convectional full adder consists of mainly three steps: They are:

1. S-Edit(schematic)
2. L-Edit(Layout)
3. LVS(Layout Vs Schematic) A.

S-EDIT:

The steps involved in designing the schematic are mentioned below.

First we have to create a new folder. Go to file then new design in the file.

Enter the project name at your project folder (the created new folder).

Now we have to click the library panel, add all the library files which are present in my documents.

Then we have to draw the schematic by using NMOS and PMOS and body terminals, voltage sources and print voltage which will be present at the left side of the panel which we can use readily to design the schematic in figure (2).

And then for PMOS and NMOS we have to give the technology values. For PMOS it is 1.65 and for NMOs it is 0.55 widths.

In this schematic design we can generate power delay product and power dissipation by using the sweep parameters we can reduce the pdp values. We to change their capacitors values and vdd value and the power delay product we have to calculate means we should change the voltage sources in pulse voltages

The tanner EDA signal which has both analog and digital form in this which we have synthesis the schematic and layout design of convectional full adder ,then the T-spice code is generated which we have both PMOS and NMOS will have same technological value.

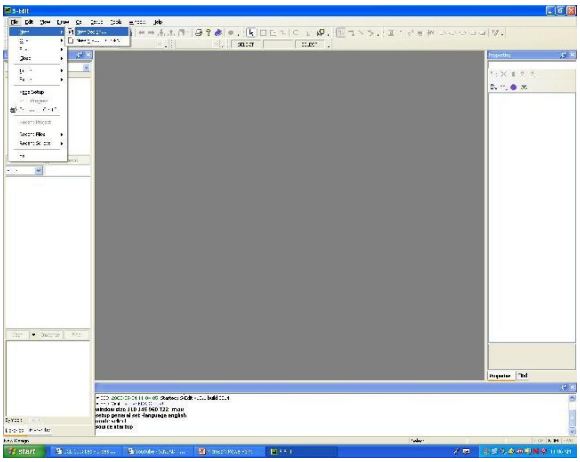


Figure 2: S-Edit of Tanner EDA

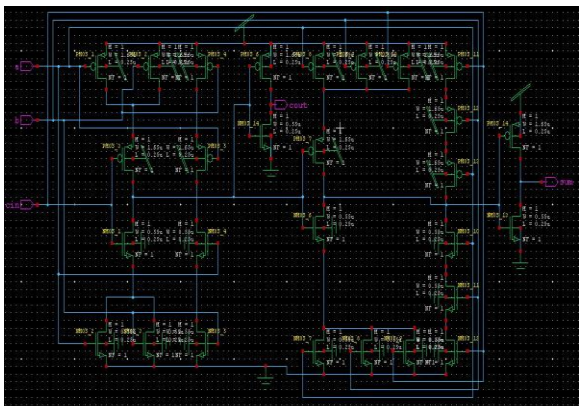


Figure 3: Schematic Diagram of 28T Full adder

Then we have to simulate the schematic , for this opens, then in the upper left we find general button click on it , in that we have to browse the project and the extension for that file should be .sp and for the resulting simulation output the output filename is filename. Out and then we have to give the stop and next time setup in transient analysis in figure (4). We have to save and run the file which then will be opened in T-spice which will be having the resultant wave form.

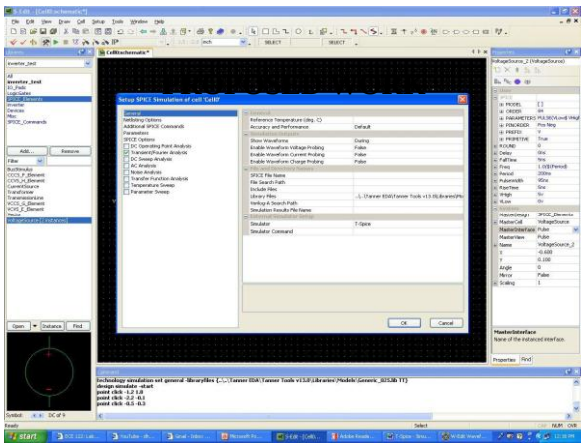


Figure 4: Attaching the Library Files of S-edit

Figure 5: Schematic Wave Form of 28T Full adder

B. LAYOUT

Depending upon the schematic the layout is being designed. In layout different colours represent different layers, For Vdd and ground we have to use metal layer which is of colour blue, and body terminal(Active) for PMOS and NMOS it is of colour green in figure (6). By connecting the PMOS and NMOS layer output can be observed which is called as polycontact which represents red colour. The combination of active and metal we have to put active contact which is surrounded by either NMOS or PMOS for PMOs we use Nselect and for NMOS we use Pselect.

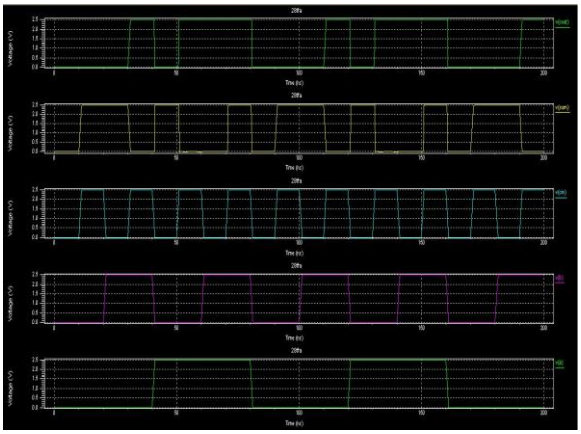


Figure 6: Layout of 28T Full adder

For to check the layout whether correct or not we have to check DRC rules and then we have to open the extract file in these we have to add library commands for L-Edit it is 0.25um MODEL_TYP.md and then we have to give the voltage sources which are similar to those given in schematic and then we have to click the transient results for which we have to give the values for inputs.

By using different layers in designing layout we have to give spacing level of each layer both PMOs and NMOs transistors and two different metals are using in this layout design that will be in blue colour and grey colour. Here we are using number of transistors power dissipation should increase and the number transistors which we are decreasing the transistors will reduce the power value.

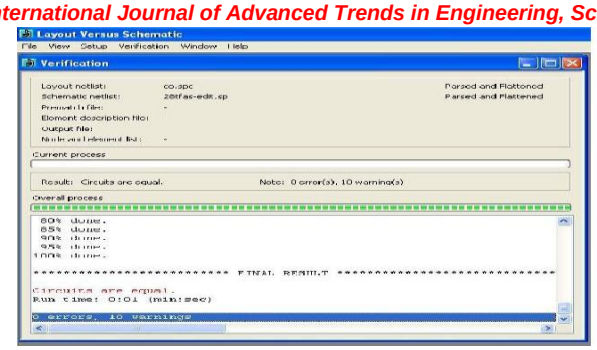
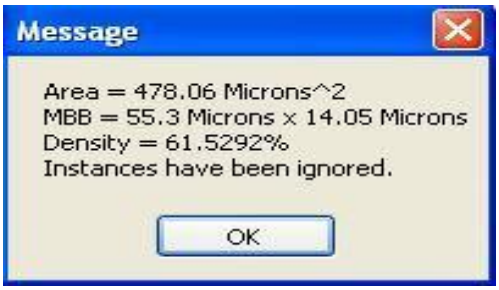


Figure 7: Layout of 28T Full adder Wave Form

C. LVS

In LVS we have to compare the Layout of T-Spice code and Schematic T-spice code both inputs and outputs should be equal and even the length and width also should be equal which shows in figure (8).

In L-Edit we have to calculate the area which is available in L–Edit tool bar.



So area=478.06 µm²

By using S-Edit we have to calculate Power, Delay, and Power Delay Product (PDP).by considering the stimulation results table-3 the average delay for a-s, b-s, cin-s inputs is 3.8513125e-009 and for a-co, b-co, cin-co inputs is 3.7434375e-009. The propagation delay for the averaged value of inputs is 3.795e-009 delay the final value is power delay product (PDP), which is about 1.42j.by using these values we have change in schematic capacitor values has Cl=1pF, Vdd=2.5v.

VII. CONCLUSION

The paper presents design and implementation of CMOS full adder using fully static logic design style which is most suitable for low-energy applications. Also the realization of CMOS full adder gives even better calculation of Power Delay Product by using 0.25µm CMOS technology.

REFERENCES

[1] Jayram Shrivas, Shyam Akashe, Nitesh Tiwari," Design and Performance Analysis of 1 bit Full Adder using GDI Technique in Nanometer Era", 2012 World Congress on Information and Communication Technologies.

[2] R.Uma ," 4-Bit Fast Adder Design: Topology and Layout with Self-Resetting Logic for Low Power VLSI Circuits", IJAEST, Vol No. 7, Issue No. 2, 197 – 205.

[3] R.UMA,Vidya Vijayan, M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", VLSICS, Vol.3, No.1, February 2012.

[4] Arvind Kumar, 2Anil Kumar Goyal," Study of Various Full Adders using Tanner EDA Tool", IJCST Vol. 3, Iss ue 1, Jan. - March 2012.

[5] Attapon Sudsakorn, Siraphop Tooprakai , Kobchai Dejhan, "Low Power CMOS Full Adder Cells".

[6] http://www.tannereda.com.

[7] Study of Various Full Adders using Tanner EDA Tool1Arvind Kumar, 2Anil Kumar Goyal1,2Dept. of ECE, UIET, Panjab University, Chandigarh, UT, IndiaIJCST Vol. 3, Iss ue 1, Jan. - March 2012

[8] Design and Simulation of Low power CMOS Adder at 180nm using Tanner Tool International Journal of Computer Applications (0975 – 8887) Volume 62– No.16, January 2013 Design of Area and Power Efficient Modified Carry Select Adder International Journal of Computer Applications (0975
– 8887) Volume 33– No.3, November 2011