An optimized array multiplier using universal logic circuits

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Abstract:***Digital signal and image processing algorithms uses multipliers, as prominent circuit. If multiplier is implemented with less delay, the corresponding algorithm can be implemented with less delay. Generally Multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit called binary multiplier. It is an electronic circuit used in digital electronics such as computer. Designing of multipliers that are of high speed and low power are of substantial research interest. Speed can be increased by reducing the generated partial products. The major concern for the VLSI circuit designers is to achieve high speed integrated circuits with low power consumption. In general, an array multiplier circuit contains the set of AND gates, FULL ADDERS and HALF ADDERS. An n×n multiplier can contain 'n (n-2)' full adders, 'n' half adders, $'n^2{}'$ AND gates. In an array multiplier worst case delay would be (2n+1)t_d, and summands are produced by the AND gates. In this project, a modified full adder and half adder using universal logic circuits are proposed to achieve low power consumption of an array multiplier. So that, high speed and low power multiplier is implemented. The designs are developed using Verilog HDL and the functionalities are verified through simulation using XILINX.***

Keywords:*Array multiplier, adders, universal logic circuit, partial products.*

I. INTRODUCTION

A Multiplier is one of the key hardware block plays an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets. They are high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. The composition of an array multiplier consists of one to one topological correspondence between this hardware structure and the manual multiplication. The generation of n partial products requires N*M two bit AND gates. Most of the area of the multiplier is devoted to the adding of n partial products, which requires N-1, M-bit adders. The shifting of the partial products for their proper alignment's performed by simple routing and does not require any logic. The overall structure can be easily be compacted into rectangle, resulting in very efficient layout.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents

different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier.

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, and area and power consumption. The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. a multiplier of size n bits has n^2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs.

II.REVIEW OF LITERATURE

1. Array multiplier

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm as shown in figure.1. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder.Multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. In array multiplier, consider two binary numbers A and B, of m and n bits. There are summands that are produced in parallel by a set of an AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n^2 AND gates. Also, in array multiplier worst case delay would be $(2n+1)t_d$.

2. Full adder

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and C_{in}; *A* and*B* are the operands, and C_{in} is a bit carried in from the previous less-significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output, output carry and sum typically represented by the signals C_{out} and *S*, where SUM=2*Cout+S. A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. One example implementation is with S=A XOR B XOR Cinand Cout=(A.B)+(Cin.(A XOR B)). The hardware requirement in terms of full adder (FA) and the length of final adder (FAL) for different size of array multipliers is obtained in the manner given in figure.2.

3. Conventional full adder

The conventional array multiplier uses full adder in its reduction phase. The bottleneck of full adder is high power consumption due to XOR gates. As shown in fig. 3 conventional full adder consists of two XOR gates in critical

Delay = 2 XOR

Path of sum and one XOR gate, one AND gate and one OR gate in the critical path of the carry.

4. *Mux based full adder*

In order to reduce the power and area, the conventional full adder in reduction phase of array multiplier is replaced by a modified full adder [9]. in mux based full adder the full adder is implemented using 4:1 multiplexers as shown in fig. 4. by implementing mux based full adder in reduction phase of array multiplier power reduction has been achieved. it is evident that, one 4:1 mux can be made using three 2:1 mux. the critical path delay can be written as shown below the array multiplier can be made more efficient by further reducing the critical path delay. the same can be achieved by using proposed full adder.

$$\text{Delay} = \text{NOT} + 2\ \text{MUX}$$

III.PROPOSED WORK

The proposed modified full adder circuit as shown in fig.5 consists of two 2:1 MUX and an XOR gate. In the proposed structure, one XOR block in the conventional full adder is replaced by a multiplexer block so that the critical path delay is minimized.

This can be implemented by using second MUX with XOR output as selection line. Since XOR employs most of the power consumption in the adder circuit, by reducing number of XOR gates, power consumption of the full adder can be reduced. The proposed full adder is applied into array multiplier reduction stage to validate the effectiveness. In array structure the partial products is divided into certain levels. In each level, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement is provided as inputs to the first multiplexer. The other two inputs are given to XOR gate, the output of which will act as a select line to both the multiplexers. The inputs of the second multiplexer are, the bits other than the carry bit as shown in figure.1. This unique way of designing leads to the reduction of the switching activity, which in turn reduces the power. In addition to this, the critical path delay is also reduced compared to the existing designs discussed in literature, which leads to reduction in delay and thus increasing the speed. Operation of the proposed full adder can be explained as follows:

- When both B and C are zero or one, sum = A;
- When either of B or C is one and another is zero, sum=A;
- When both B and C are zero or one, carry= B;
- When either of B or C is one and another is zero, carry= A; l.

IV.RESULTS

The proposed and the existing multiplier designs are developed using Verilog HDL for 8 and 16 bits, respectively. The functionality of the 32-bit proposed array multiplier is verified through simulations using Quart us tool. The simulation waveform of array multiplier using proposed full adder for 8-bits is shown in fig.6. All the multiplier designs are synthesized in Synopsys Design Compiler using SAED90nm CMOS technology. As the synthesized results indicates an average power reduction of 29.94% for 8-bit and 44.97% for 16-bit respectively, compared to existing multiplier architectures. The average area reduction of 45.38% for 16-bit and 46.13% for 32-bit are also achieved. The average delay is also reduced by 11.8% for 16-bit and 29.45% for 32-bit compared to the existing architectures.

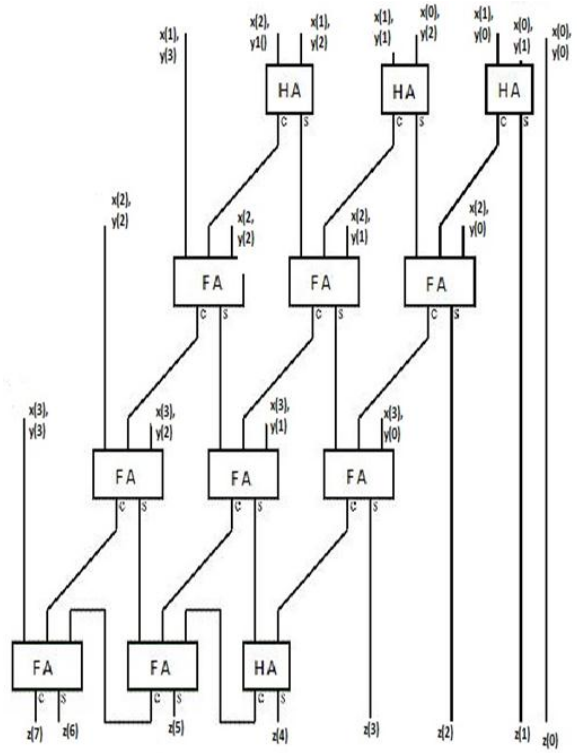

Figure1. An array multiplier

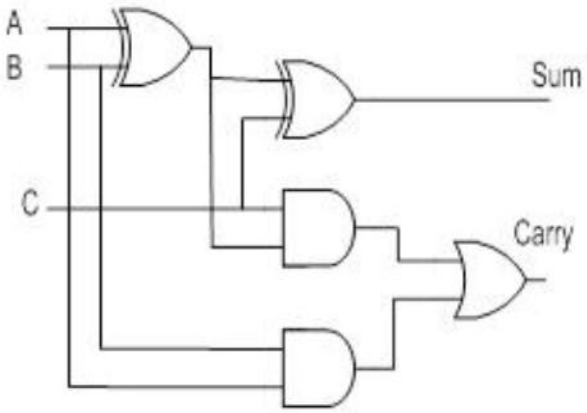

Figure1.Full adder

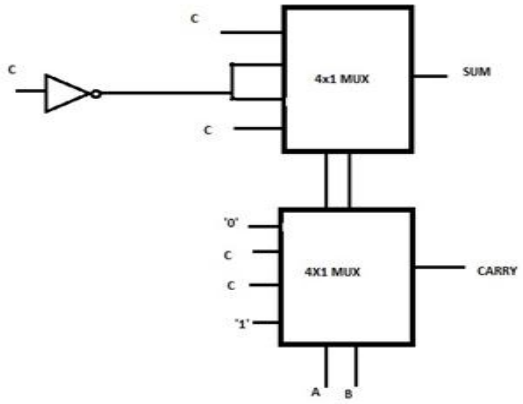

Figure3. Universal logic circuit based Full Adder

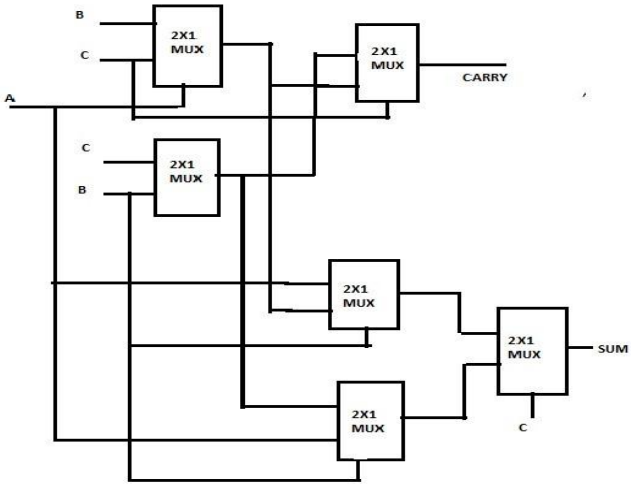

Figure4.Full adder using six Universal logic circuit

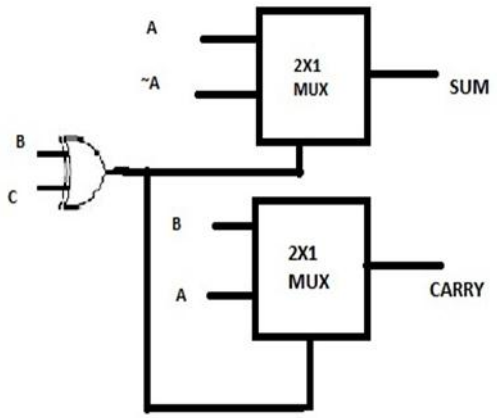

Figure5. Proposed full adder

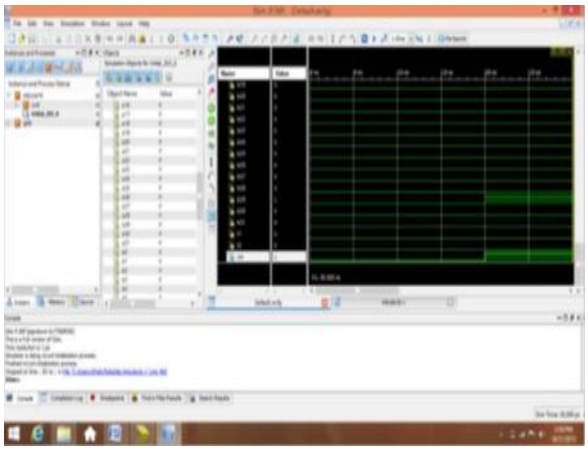

Figure6. simulation of 32 bit array multiplier

V. CONCLUSION

In this paper, a modified full adder using universal logic circuits and XOR gate is proposed. By incorporating the modified full adder in the reduction stage of Wallace tree multiplier, an average power, area and delay reduction of 35.45% ,40.75% and 15.65% respectively, compared to existing methods respectively is achieved. The synthesis result confirms that the proposed Wallace tree multiplier is suitable for low power and small area applications

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BIOGRAPHY

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