Design and analysis of Clocked Regenerative Comparators –Case study

R. Mahesh Kumar[1],
[1]Asst. Professor,
Dept of ECE,
AITS, Rajampet.
r.mahesh.1021@gmail.com

N.Bala Dastagiri[2],
[2]Asst. Professor,
Dept of ECE,
AITS, Rajampet.

B.Abdul Rahim[3],
[3]Professor
Dept of ECE,
AITS, Rajampet.

S.Fahimuddin[4]
[4]Assoc. Professor
Dept of ECE,
AITS, Rajampet.

ABSTRACT

Clocked Regenerative comparators plays a crucial role in the design of ADCs in terms of high speed and low power.IN this brief various clocked regenerative latched comparators are designed and analysed for their power dissipation and delay. Also its transient response is plotted. It is shown that a comparator with speed as priority suffers high power dissipation and vice-versa. The designs are simulated using 130nm CMOS technology using Mentor Graphics tools.

KEYWORDS

Clocked Regenerative Comparators, Power Dissipation, Delay, ADCs.

I.INTRODUCTION

With the advent of new technologies in the field of electronics, major importance is given towards the application with high speed and low power dissipation. Speed, lower power dissipation, low noise, better slew rate, resolution are the important features of high speed applications such as sense amplifier, SOC design, data links etc. In order to fulfil these specifications the basic building i.e. comparator has to be tightly constrained. Hence design of comparator is more challenging [1].

A comparator compares a differential input signal with a predeterminedthreshold voltage and gives a digital output accordingly [7]. To design a comparator with speed as priority the number of transistors required will be more which indeed increases area, power and supply voltage. One efficient method is to design a regenerative stage in the pre-amplified based regenerative comparator. For a design with low power dissipation as a priority reduction in speed occurs with increase in transistor count as in dynamic latched comparators at the expense of high offset voltage [2][3].Because such comparator topologies do not have static pre-amplification in the front of a latch part, thus have unavoidablylarge offset voltages. The offset of a comparator can be defined by additional differential input signal to the ideal differential input to achieve adesired output. Offset voltage affects the accuracy of the circuit. In order to achieve an optimum comparator design, it isessential to have accurate methods to predict offset voltages [6].

From the above discussions comparators are likely to be classified into the following types.

i. Open loop comparators
ii. Regenerative comparators
iii. Fully dynamic latched comparators

In this paper the above mentioned comparators will be designed and their performances were compared w.r.t power, propagation delay and speed.
This paper is organized as follows. In section II, preamplifier based comparator, conventional dynamic comparator, resistor divider dynamic comparator, double tail dynamic comparator are designed. In section III, various comparators are simulated for their operating principles and the analytical work is compared. In section IV the work mentioned is concluded.

II. DESIGN OF CLOCKED COMPARATOR ARCHITECTURES:

2.1 Pre amplifier based comparator:

This comparator has the three stages in which are shown in fig. 3.1. i.e.,

- Input pre amplifier stage
- Latch stage or regenerative stage
- Output buffer stage

Pre amplifier stage has a differential amplifier with active loads. The pre amplifier stage amplifies the input signal to improve the comparator sensitivity.

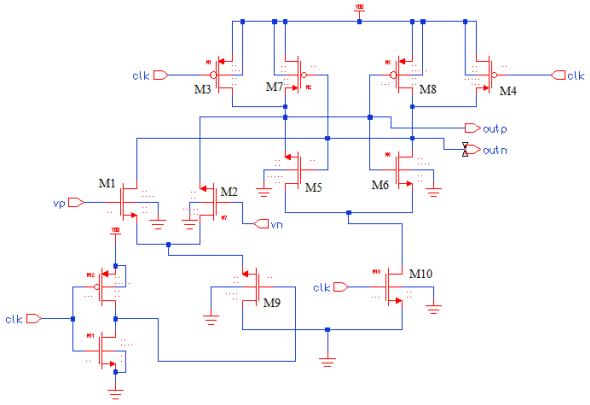

Fig-1: Pre-amplifier based dynamic comparator

The latch stage has provides the positive feedback and is used to obtain which of the input signals is larger and amplifies their difference. This stage is comprised of the transistors M5– M8 and M10. The circuit works in two phases, i.e. amplification phase and the regenerative or evaluation phase. During the CLK=0 (amplification phase), the tail transistor M9 turns ON and M10 turns OFF. This amplification stage is also capable to produce its output close to VDD-|Vthp| which can effectively reduce the charging time. In this stage Vp-Vn is amplified and given to regenerative stage. When the clock CLK=1 (regeneration phase), M10 turns ON and M9 turns OFF.

There is a provision to minimize the delay in the pre-amplifier based clocked comparator over the other latched comparators. However, the pre-amplifier based clocked comparator consumes static power during the amplification period and also the energy consumption in the pre-amplifier based clocked comparator becomes more than the other latched comparators. But the preamplifier based comparators suffer not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance rds due to the continuous technology scaling There is a reduction of the power dissipation in the double tail latch comparator over the pre-amplifier based clocked comparator.The output buffer stage consisting of a self-biased differential amplifier which is followed by an inverter and it converts output of a latch stage to a full scale digital level output (1 or 0). This stage should accept a differential input signal and do not have limitations of slew rate.

2.2. Conventional single tail dynamic latch comparator:

The schematic circuit of the conventional dynamic latch comparator is shown in fig.3.2 which offers high impedance, rail to rail output swing and zero static power dissipation. The operation could be takes place in two phases i.e. Reset (precharge) and comparison (evaluation) phase. During the reset phase (CLK = 0), Mtail Transistor is off, reset transistors (P1–P4) pulls both the output nodes (Outn and Outp) to VDD which defines a start condition and to have a valid logical level during reset.During the comparison phase, when CLK = VDD or 1, transistors P1 and P4 are off, and Mtail will be on then the Output nodes (Outp&Outn), which had been precharged to VDD, then these node capacitors start dischrges depending on the applied input voltage at VINN and VINP. Let us consider the case when VINP > VINN, then the node capacitor at Outp discharges faster than the node capacitor at Outn. Hence when Outp (discharged by transistor N4 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor N1 drain current), the corresponding pmos transistor (P2) will turn on initiating the latch regeneration caused by back-to-back inverters (N2, P2 and N3, P3). Thus, Outn pulls to VDD and Outp discharges to ground.

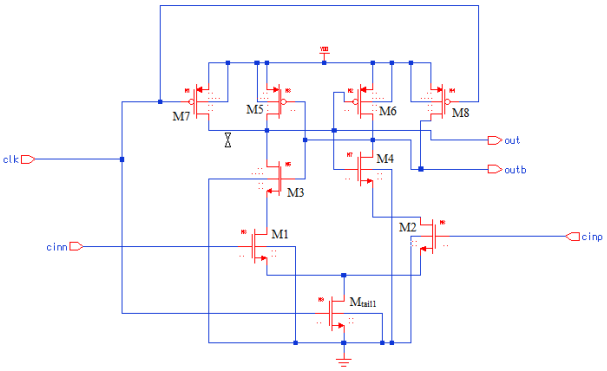

Fig-2: Conventional single tail dynamic comparator

2.3. Conventional double - tail dynamic latch comparator:

A conventional double-tail dynamic latch comparator is shown in Fig.3.3. This comparator has less stacking of transistors and therefore it can be operate at lower supply voltages compared to the conventional single tail dynamic latch comparator. This comparator is much similar operation as discussed in previous comparator with two phases i.e. pre-charge phase and evaluation phase. During reset phase (CLK = 0), Mtail1, and Mtail2 are off, transistors M3-M4 pre-charged and the nodes(outp and outn) pulls to VDD, which in turn affects transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase or evaluation (CLK = VDD), Mtail1 and

Mtail2 turn on, M3-M4 turn off and voltages at nodes outn and outp start to down with the rate defined by imtail1/COUTN(p) and moreover, an input-dependent differential voltage Voutn(p) will build up. The stage which is formed between the MR1 and MR2 passes Voutn(p) to the cross-coupled inverters and also

protection between input and output, which results in reduction of power and delay.

The voltage difference at the final stage outputs at the initial delay time has a profound effect on latch initial differential output voltage and consequently on the latch delay. The disadvantage of this dynamic comparator is both the intermediate transistors will be cut-off; hence they do not have importance to improving the efficient transconductance of inverter latch. In addition, during reset phase, these nodes need to be charged from ground to V_{DD} which is difficult to achieve.

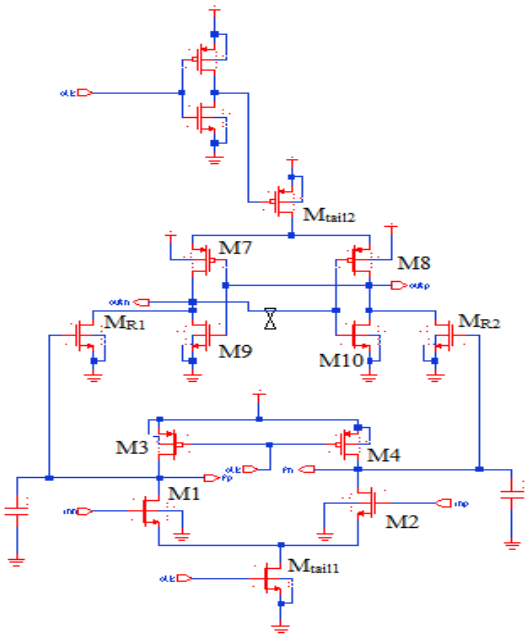

Fig-3: Conventional double tail dynamic comparator

2.4 Resistor divider dynamic comparator (Lewis-Gray structure):

The schematic circuit of the comparator is shown in fig.3.4. This comparator is widely used in pipeline type of Analog to Digital Converters. The input transistors M1and M2 will be operated in the triode region and these transistors behaves like voltage controlled resistors. The major merit of this comparator is lower power consumption and decision level threshold voltage adjustment is possible. However, resistor divider dynamic comparator can exhibit high offset voltage, this voltage is depends on different common mode voltage *Vcom*, and it is only applicable for low resolution comparison.

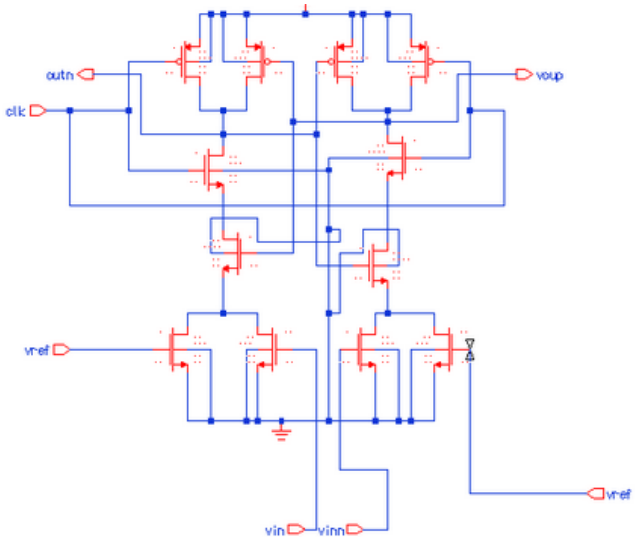

Fig-4 :Resistor divider or lewis-gray dynamic comparator

III. SIMULATON RESULTS AND COMPARISION

This section analyses the various performances and compares the different comparators discussed above. These circuits were simulated using Mentor Graphics EDA Tool with 130nm CMOS technology. A comparision table is noted based on the speed, propagation delay and power dissipation. Also the transient responses were plotted.

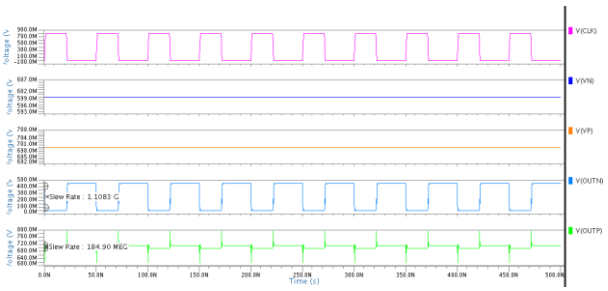

Fig-5: Transient response of Pre-amplifier based dynamic comparator

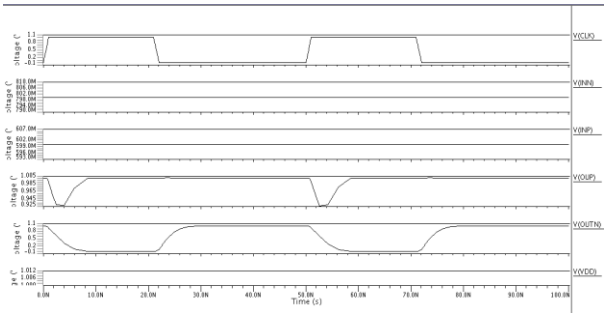

Fig-6: Transient response of Sinlge tail dynamic

comparator

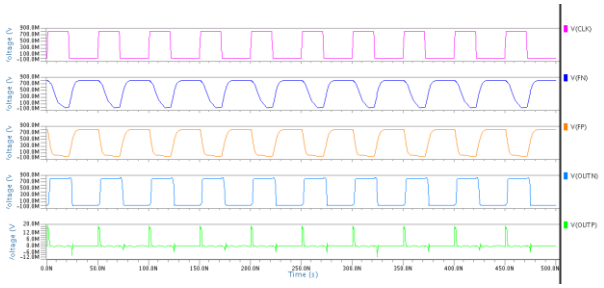

Fig-7: Transient response of double tail dynamic comparator

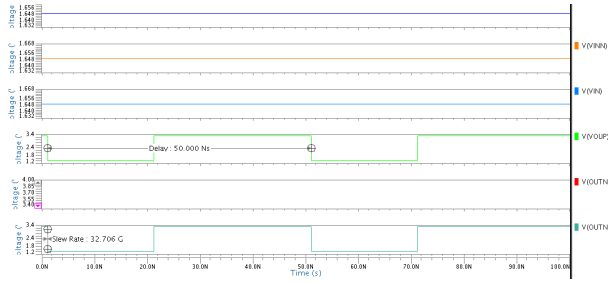

Fig-8: Transient response of resistor divider dynamic comparator

PERFORMANCE COMPARISON:

COMPARATOR TYPE	POWER (W)	DELAY (NS)
Pre- amplifier	175.7429 µ	0.013
Single tail dynamic comparator	93.4N	0.019
Double tail dynamic comparator	1.282N	0.034
Resistor divider dynamic comparator	1.5458N	0.018

IV.CONCLUSION

In this paper, the analysis of power consumption and delay for different structures of clocked comparators were presented by using 130nm CMOS technology. Based on the designs we can note that power dissipation is more if speed taken as the priority and vice-versa.

REFERENCE

[1]. N. Naga Sudha#1, V. Narasimha Nayak#2, SuneelMudunuru*2,M. Nagesh Babu#3,B.K.V Prasad#4, M. Jyothi#5,High Speed and Low Power Dynamic Latched Comparator for PTL Circuit Applications, International Journal of Computer Science and Information Technologies, Vol. 3 (1) , 2012, 2982 – 2991

[2]. Vinotha V1, Menakadevi B2, Design of Low-Voltage, Power Proposed DynamicClocked Comparator, International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 3, Issue 1, January 2014

[3]. Chandrahash Pate1, Dr.Veena C.S.2, Prof.Shivendra Singh, *international journal of innovative research in electrical, electronics, instrumentation and control engineering vol. 2, Issue 8, August 2014*

[4]. Jun He, Sanyi Zhan, Degang Chen, *Senior Member, IEEE,* and Randall L. Geiger, *Fellow, IEEE,* Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators, IEEE transactions on circuits and systems—i: regular papers, vol. 56, no. 5, may 2009

[5]. D.Nageshwar Rao1, M.S Sameera2, M D.Nizamuddin Salman3, Zubeda Begum, Design of Low Power High Speed Fully Dynamic CMOS Latched Comparator, International Journal of Engineering Research and Development *e-ISSN: 2278-067X, p-ISSN: 2278-800X, www.ijerd.com Volume 10, Issue 4 (April 2014), PP.01-06*

[6]. Neerav Mehan1, Anshul Kumar2, Kamna Kohli3, Neha Sharma, Offset Reduction of CMOS Based Dynamic Comparator by using Charge Storage Techniques - A Comparative Study,