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Systematic Design of High-Speed and Low-Power Domino Logic

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***Abstract:** Dynamic Domino logic circuits are widely used in modern digital VLSI circuits. Because it is simple to implement, low cost designs in CMOS Domino logic are presented. Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in logic such as domino circuits is used in high-performance applications. Domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates. This paper compares static CMOS, domino logic design implementations. For the comparison of static CMOS and DOMINO logic we will see various design of Domino logic gates and as well as design of logic circuits using Domino logic gates.*

***Keywords** – Dynamic; Domino; CMOS; Very Deep submicron technology; High speed; Low Power.*

I. INTRODUCTION

Dynamic circuits are widely used in custom circuit design to achieve higher speed, smaller area and potentially lower power consumption due to glitch -free operation. There are also difficulties in designing and verifying this class of circuits However, Domino logic circuits can implement only non-inverting logic; the synthesis of a Domino logic circuit typically involves the conversion to a unate representation from the original binate logic network. Synthesis of domino circuits is more complicated than that of static circuits. The added complexity is due to domino log ic's monotonic nature which forces it to implement only non-inverting functions. Therefore, domino logic can only be mapped to a network of non-inverting functions, where needed logic inversions must be performed at either primary inputs and/or primary outputs. Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow P transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice. There are also difficulties in designing and verifying this class of circuits. Dynamic circuitry can become highly sensitive to clock skew, charge sharing etc. Do mino logic has created a substantial interest due to its performance and CMOS power consumption. It runs 1.5 - 2 times faster than static CMOS logic because dynamic

II. RELATED WORK

Dynamic logic (or sometimes clocked logic) is a design methodology in combinational logic circuits, particularly those implemented in standard CMOS logic .Standard CMOS logic has the disadvantages of increased area, complexi-ty and delay. Standard CMOS logic is built on transistors. The input is same to both the PMOS and NMOS transistors.

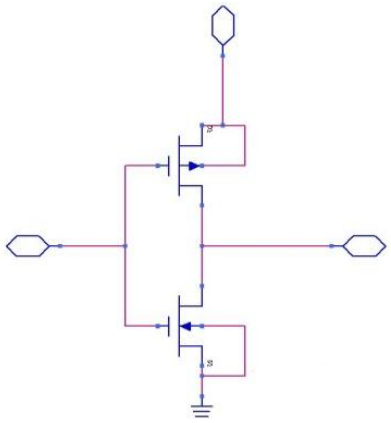

Fig: CMOS Inverter

Simulation results

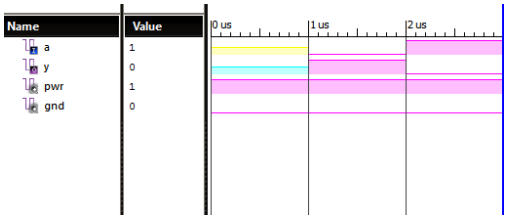

Fig:2 CMOS inverter

To overcome the disadvantages of CMOS logic the alternate forms are discovered. Now the pseudo inverter is used.

The inverter that uses a p-device pull-up or load that has its gate permanently ground. An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is NMOS technology and is called pseudo NMOS logic. In this the PMOS is always connected to ground and depending on the input of NMOS transistor the output goes high or low. The PMOS is shown in figure

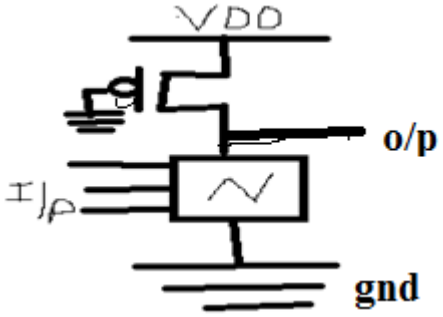

Fig: pseudo NMOS gate

The disadvantages of pseudo NMOS logic are static current flow between vdd and vss and high power consumption. To overcome these disadvantages dynamic CMOS logic is invented.

A dynamic CMOS circuits rely on the temporary storage of signal values on the capacitance of high- impedance circuit nodes. These circuits also have no ststic power dissipation and uses a sequence of pre-charge and conditional evaluation phases with the addition of a clock input.

The dynamic CMOS logic is shown in the figure.

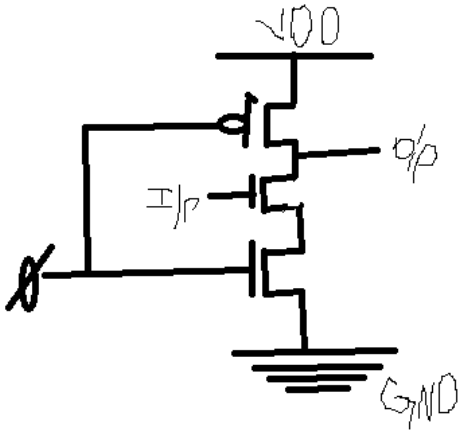

Fig: dynamic CMOS logic

A dynamic CMOS logic uses charge storage and clocking properties of mos transistors. In dynamic logic we have an clock which determines the phase. This dynamic CMOS circuit has serious problem when they are cascaded. This can be by connecting a inverter at the output.

III.PROPOSED WORK

Domino CMOS logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to- rail logic swing. It is developed to speed-up-circuits. It is slightly modified version of the dynamic CMOS logic circuit .in this case a static inverter is connected at the output of each dynamic logic block. The addition of the inverter solves the problem of cascading of dynamic CMOS circuit.

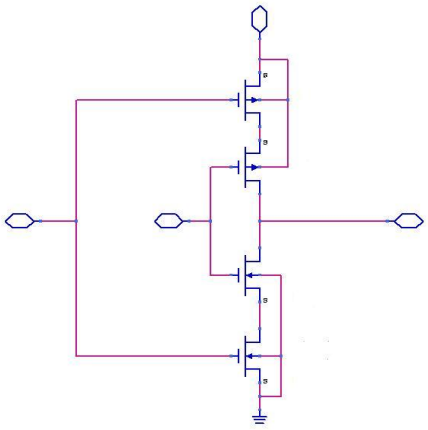

Fig: domino inverter

Simulation results

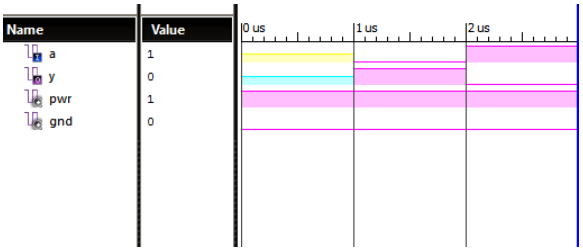

Fig: domino logic

domino logic consists low power consumption. These non-inverting structures are possible because of presence of inverters. When compared to standard CMOS logic area, complexity, and cascading problem of dynamic CMOS logic are reduced.

IV CONCLUSION

This paper has presented a design methodology for Domino logic circuits. Domino Logic circuits have become extremely popular in the design of today's high performance processors because they offer fast switching speeds and reduced areas. In this paper, comparison of CMOS Logic circuits and DOMINO Logic circuits of various design of Domino logic gates and as well as design of logic circuits using Domino logic gates have been explored. In this work, an attempt has been made to simulate AND gate, Fu ll adder by using the proposed techniques. Domino circuits have offered an improved performance in speed and power when compared with CMOS circuit. As it is observed from the results that Do mino circuits offer better solution for the low power and high speed than CMOS circuits. Hence, it is concluded that the proposed design of DOMINO Logic will provide a platform for designing high performance and low power digital circuits

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