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Adder Enhancement Techniques

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***Abstract:** Adders are one of the most widely digital components in the digital integrated circuit design and are the necessary part of digital signal processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. The addition of the two bits is very based on the various speed-up schemes for binary addition, a comprehensive overview and qualitative evaluation of the different existing basic adder architectures are given in this paper. In addition , their comparison is performed in thesis for the performance analysis. We will synthesize the adders –Ripple Carry adder, Carry skip adder, Carry select adder and Carry look –ahead Adder, in ISE XILINX 13.2 by using HDL - Verilog and will simulate them in same tool. We will compare above mentioned adders in terms of delay, Slices Used and Look up tables used by the adders architecture.*

Key words :Ripple Carry Adder, Carry Look Ahead adder, Carry Save adder

INTRODUCTION

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.[1]

This paper presents a comparative analysis of various adders and comparison in terms of area and delay

RIPPLE CARRY ADDER

A ripple adder that adds two N-bit operands requires N full adders. The speed varies linearly with the word length. The RCA implements the conventional way of adding two numbers. In this architecture the operands are added bitwise from the least significant bits (LSBs) to the most significant (MSBs), adding at each stage the carry from the previous stage.

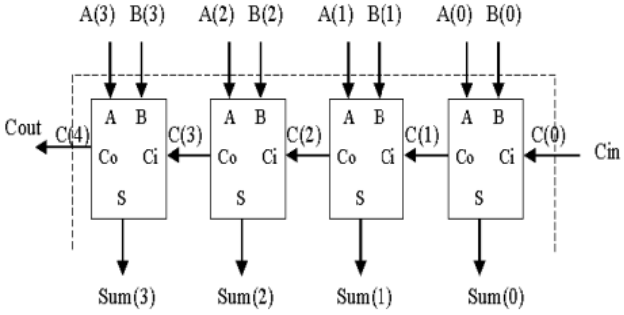


Fig : 4-bit Ripple Carry Adder

Thus the carry out from the FA at stage i goes into the FA at stage (i +1), and in this manner carry ripples from LSB to MSB (hence the name of ripple carry adder). The layout of a RCA is simple, which allows fast design time. However, RCA is relatively slow, since each full adder must wait for the carry bit which is coming from the

previous full adder

CARRY SKIP ADDER

CSA uses some setup to block the carry propagation. In a setup if the bits of the two operands are different in all the positions with respect to each other then carry need not to be generated . Hence in such cases the carry need not be propagated through the adder block. Instead the previous carry can be directly transmitted through a multiplexer to the next block.

If the bits of the operand are not different in any one position then previous carry needs to propagate through the adder block .

In carry skip adder if the bits of the operands satisfies Ex-or condition in all the positions then it works as a carry bypass adder, otherwise it works as a normal ripple carry adder. It means that in this adder the carry bypassing is depends on the data of the operands. So we have to move to the other adders like carry select adder to overcome this dependency.

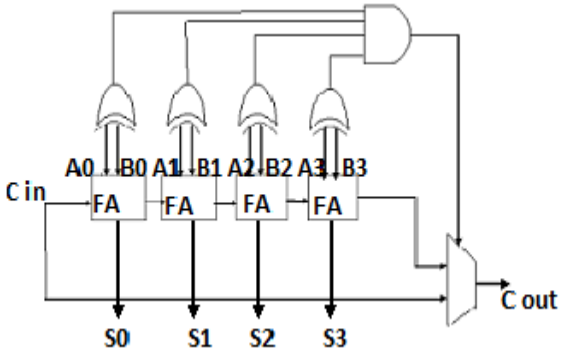


Fig: Basic Carry Skip Adder

CARRY SELECT ADDERS

Carry select adder is a fast adder which is used in digital communication and Memory Architectures. The Carry of one ripple carry adder will be '0' and another will be '1'.Here the output sum and carry is identified by the 2 to 1 multiplexers .

The control signal of the multiplexer is carry C_{IN}.

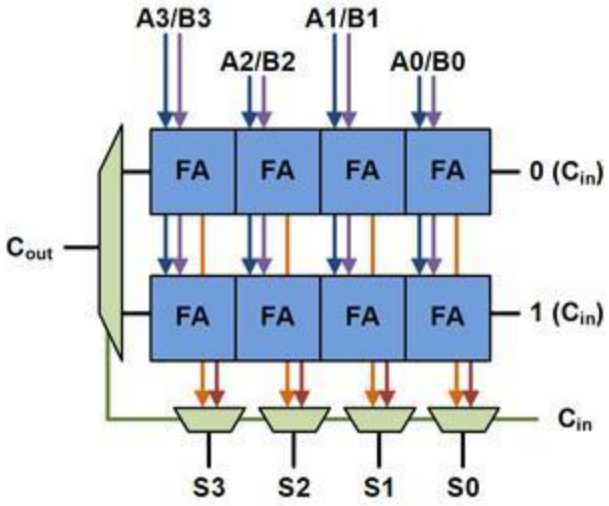


Fig Basic Carry Select adder circuit

The carry select adders are divided into two types: Uniform Sized Adders and Variable Sized Adders. If the bit length is equally divided it is called Uniform Sized adders. It is also called Linear Carry select adder. In Variable Sized Adders the bit length are unequally divided as given in Fig.2. It is also called SQRT carry select adder (CSA). Normally the CSLA is designed with the Dual Ripple Carry Adders with the carry being '1' and '0'.Here instead of having Dual ripple carry we are having only single Ripple carry Adder while the Binary to Excess one converter is connected instead of RCA with Carry '1'

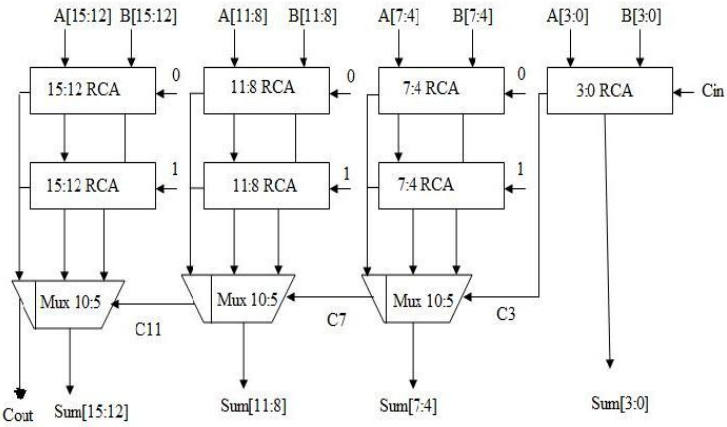


Fig. 16-bit conventional carry select adder

CARRY LOOK-AHEAD ADDER

It is a synchronous addition which was introduced by Wienberger & Smith in 1956. It is

based on the principle that even if the number of input is increased the carry propagation can be still reduced. Its concept is to propagate the carry as fast as possible to the last stage for all operand values .

In the CLA adder carry generation signal and carry propagate signals are generated. A carry is generated when both inputs A and B are '1'. Carry is propagated when any of the input A or B is '1'.

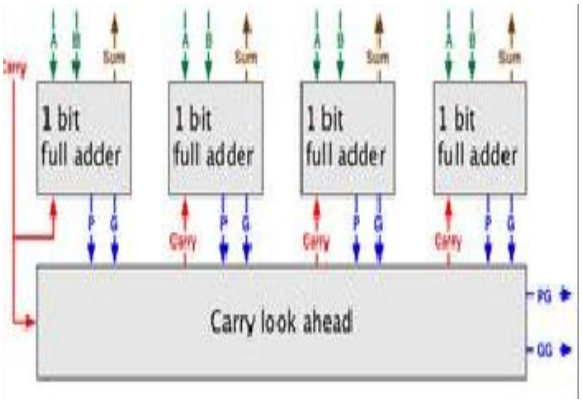


Fig: 4-bit carry look-ahead adder

Equations of Full adder are
C = A.B + B.C + C.A = A.B+ C(A+B)
The above expression can also be written as
C = G+P.C
And
C i+1 = Gi + Pi Ci
Now
C0 = G0 + P0.Cin
C1 = G1 + P1 G0 + P1 P0 .Cin
C2 = G2 + P2 . G1 + P2 . P1 . G0 +P2 . P1 . P0 . Cin
C3 = G3 + P3.G2 + P3.P2.G1 + P3.P2.P1 .G0 + P3.P2.P1.P0.Cin
Cn+1 = Gn + Gn-1.Pn + Gn-2.Pn.Pn-1 +……+ G0.PnPn-1…P1 + PnPn-1 …P1P0Cin
One of the most popular methods to reduce delay is to use a carry look-ahead mechanism. By using carry look-ahead mechanism, the propagation delay is reduced to four-gate level irrespective of the number of bits in the adder

Fig: 16 Bit Ripple Carry adder

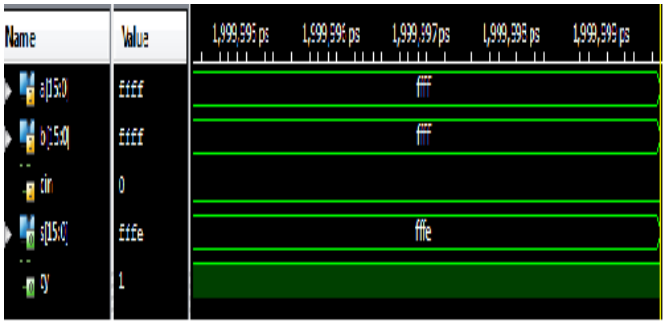


Fig: 16-bit Carry Skip Adder

Fig: Carry Select Adder

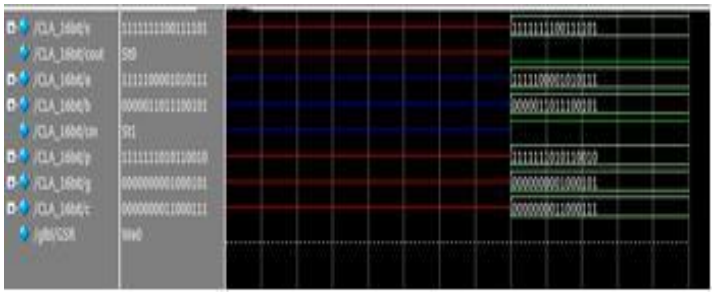
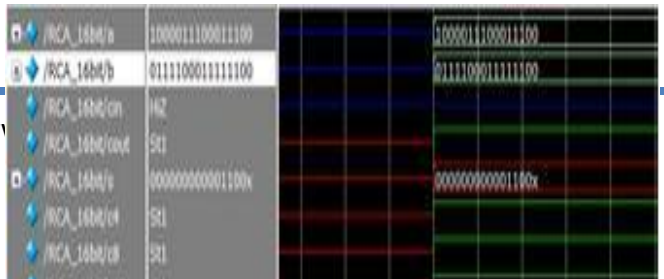


Fig: Carry Look-Ahead adder

SIMULATION RESULTS



CONCLUSION

Logic Utilization	RCA	CLA
No.of Slices	24	18
Number of 4 input LUTs	32	32
Number of Bonded IOBs	50	50
Delay	24.686ns	24.686ns

Simulation of different adders are done in Xilinx 13.2ISE design tool and by the results it can be note that CLA is the faster adder among all the adders by scarifying the area

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