New Design Of High Force WTM For VLSI Chip Applications

1.Bogati Vijaya Bhaskar Reddy,PG Student,2.Dr.C.B Reddy,Professor&HOD
1,2.Department of VLSI System Design, St .Mary's Group of Institutions, Hyderabad, India.
vijay.bogathi@gmail.com

Abstract: ***In figuring, particularly advanced sign preparing, the multiply–accumulate operation is a typical step that registers the result of two numbers and adds that item to a collector. The equipment unit that performs the operation is known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is additionally frequently called a MAC. Power dispersal is a standout amongst the most essential configuration targets in coordinated circuit, after rate. Advanced sign handling (DSP) circuits whose principle building square is a Multiplier-Accumulator (MAC) unit. Rapid and low power MAC unit is attractive for any DSP processor. This is on account of pace and throughput rate are dependably the worries of DSP framework. Macintosh unit comprises of snake, multiplier, and an aggregator it safeguards a remarkable mapping in the middle of data and yield vector of the specific circuit. In this MAC operation is performed in two sections Partial Product Generation In the proposed plan, we are utilizing Modified Wallace tree multiplier which lessens the equipment many-sided quality. As the proposed framework requires less number of assets, we enhance the force utilization. In this anticipate, another MAC is planned in view of altered Wallace tree multiplier alongside Multi operand snake.***
Key Words: Modified Wallace duplication, gathering, CSA.

I.INTRODUCTION

For a significant number of the DSP and video handling applications the multi-info expansion is an imperative operation. Utilizing trees of convey engender adders multi-info expansion has generally been actualized on FPGAs. Since to compressor trees the customary lookup table that is LUT structure of FPGAs is not manageable so due does that thing this methodology has been utilized as a part of ASIC innovation and these likewise used to actualize parallel augmentation and multi-information expansion. To guide compressor trees onto the general rationale of a FPGA we built up an insatiable heuristic in this technique. To plan parallel multi operand adders for ASIC executions albeit repetitive expansion is broadly utilized, the utilization of excess adders on Field Programmable Gate Arrays been kept away from.

By and large the Binary multi operand adders are masterminded in two ways that is one in a variety of columns and the second one as in a tree-like structure. Where to decrease m operands into a last one every column of adders lessens one further operand in an exhibit arrangement because of that m levels of adders are required. In a m-operand snake tree the quantity of rationale levels is either log2(m) nor log2(m) − 1 levels for a marked digit or a convey spare viper tree. The tree designs are typically favored on the grounds that however the exhibit a more normal directing the equipment expense of both setups is comparable.

Where the multiplier unit is an inescapable segment in large portions of the computerized signal preparing (DSP) applications are has including augmentations. Adjusted Wallace multiplier unit is utilized for elite computerized signal with the handling frameworks. The DSP applications incorporate a significant number of the sifting, convolution, and inward items. A large portion of the advanced sign handling techniques use nonlinear in the capacities, for example, discrete cosine change (DCT) or which can discrete wavelet changes (DWT). Since they are essentially proficient by dreary use of duplication and expansion, the rate of the Multiplication and expansion math decides the execution pace and execution of the whole computation. Increase and-gather operations are ordinary for computerized channels. Subsequently, the usefulness of the Multiplier unit empowers rapid separating and other handling run of the mill for DSP applications.

II.MODIFIED WALLACE IMPLEMENTATION

A changed Wall pro multiplier is a productive with the equipment execution of advanced circuit As Like this increasing two numbers. By and large the Wallace multipliers use numerous full adders and half adders are utilized for the diminishment stage. To lessen the quantity of fractional item bits in the Wallace multiplier we need to utilize the half adders. The many-sided quality of the multiplier depends on the quantities of half adders utilized as a part of the multiplier so in the event that we less number of half adders then many-sided quality is decreased, an alteration to the Wallace lessening is as done in which the postponement is the same with respect to the productive ordinary Wallace diminishment. The changed accumulation as half adders is lessened by expansion in the quantity of full snake In the Wallace increase.

Diminished unpredictability Wallace multiplier decrease comprises of three stages. To start with stage the N x N item grid is reworked fit as a fiddle of pyramid before going to the second stage is shaped and before the going on to the second stage. Amid the second stage the revised item grid is gathered into non-covering gathering of three as like to appeared in the figure 2, in the full viper the sign piece and two sign piece will give it into next stage

$$r_{j+1}= 2[r_i/3]+r_j \bmod 3$$

$$\text{If } r_j \bmod 3 = 0, \text{ then } r_{j+1} = 2r/3$$

On the off chance that the quality ascertained from the above mathematical statement for the colossal as the quantity of

lines in every stage in the second stage and the one of the second stage does not coordinate , at exactly that point the half snake will be utilized. The last result of the second stage will be in the tallness of two bits and passed onto the third stage. The convey engendering is accomplished in the third stage. Amid the third stage the yield of the second stage is given to the convey proliferation of the accomplished and produce at the last yield.

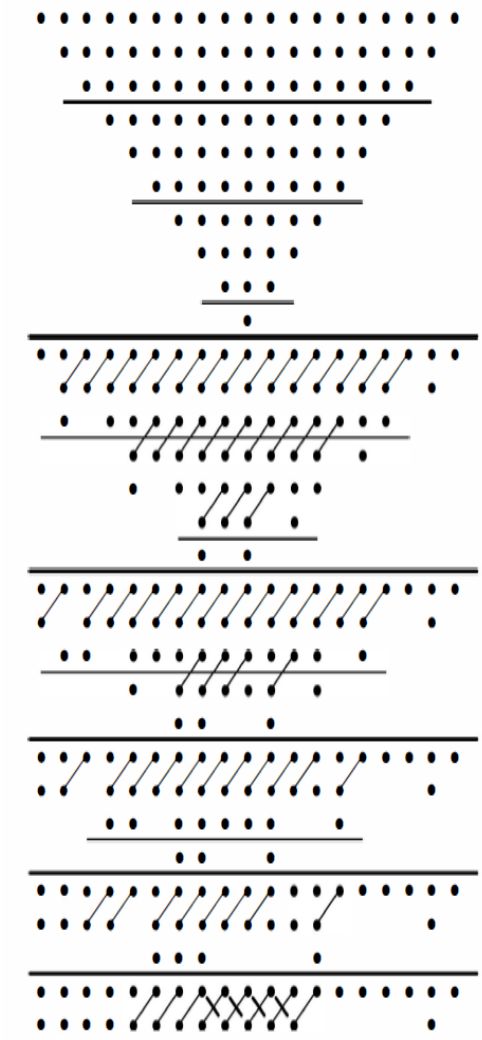

Fig.1.Modified Wallace 10-bit by 10-bit reduction.

In this way 64 bit adjusted Wallace multiplier is one of the built and the aggregate number of stages in the best second stage is 10. According to the mathematical statement the number which one of column in each of the 10 stages was ascertained and the one of the utilization of half adders was confined just to the 10thstage. The aggregate number of half adders utilized as a part of the accomplished second stage is 6 and the aggregate number of full adders that was utilized amid the second stage is somewhat with tad bit expanded that in the routine Wallace multiplier.

Since the 64 bit changed Wallace multiplier is one of the hard to speak to, a normal l0-bit by 10-bitreduction appeared in figure 2 for comprehension. The one of the accomplished extraordinary adjusted Wallace tree indicates better execution in the outline cycle when convey spare snake is utilized as a part of definite stage rather than swell convey viper. The convey spare snake which is utilized is thought to be the basic part in the multiplier since it is in charge of the biggest measure of calculation.

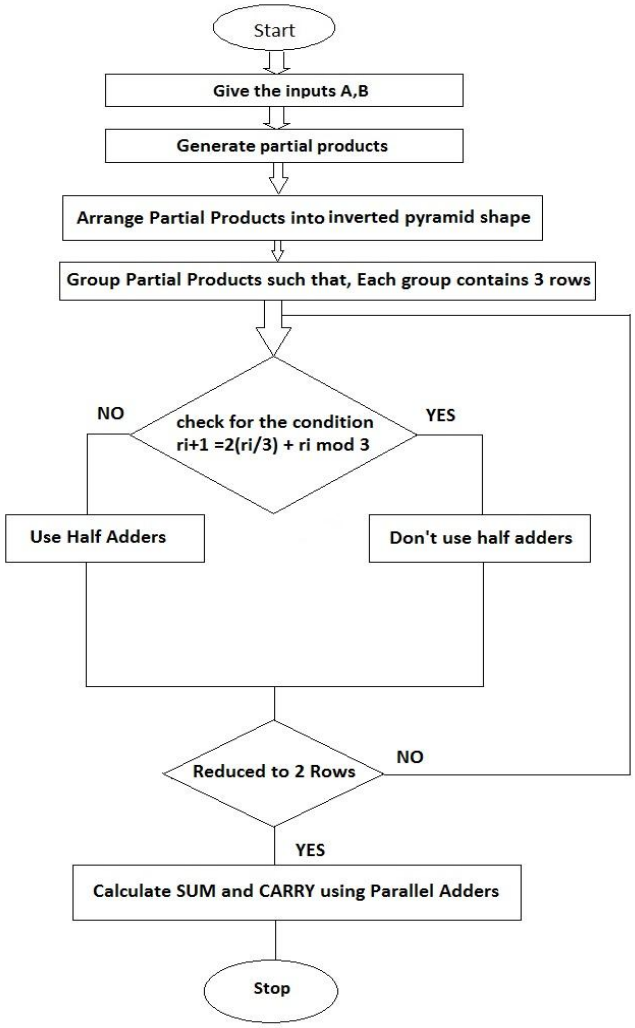

Fig.2.Flow chart for Modified Wallace Multiplier

A.Mac Operation.

The Multiplier-Accumulator (MAC) operation is the key operation in DSP applications as well as in interactive media data preparing and different applications. As said above, as like the MAC unit comprise of multiplier, snake and enlist/aggregator. In this paper, we utilized 64 bit adjusted Wallace multiplier. The MAC inputs are gotten from the memory area and given to the multiplier piece. This will be valuable in 64 bit advanced sign processor. The info which is being encouraged from the memory area is 64 bit. At the point when the data is given to the multiplier it begins processing esteem and the yield will be126 bits for the given 64 bit information and subsequently.

The yield of convey spare viper is 127 piece i.e. one piece is for the convey that is characterize as 126bits+ 1 bit. At that point, the yield is given to the collector register. In this outline is parallel in Parallel Out that is PIPO where the aggregator register utilized. All the yield values in parallel following the bits are immense furthermore convey spare snake produces, where the data bits are taken in parallel and yield is taken in parallel PIPO register is utilized. Sustained back as one of the data to the convey spare snake the yield of

the gatherer register is taken out. The figure 3 demonstrates the essential engineering of MAC unit.

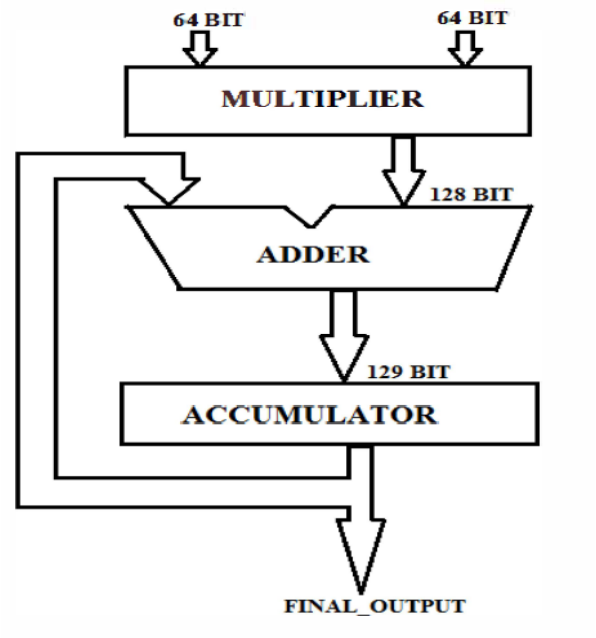

Fig.3.Basic Architecture of MAC unit.

B.Wallace Tree Multiplier

By an Australian PC researcher Chris Wallace in 1764a computerized circuit that duplicates two numbers formulated which is a Wallace tree multiplier is a proficient equipment execution. It lessens the no. of fractional items and for the expansion of halfway items use convey select snake.

In this figure blue circle speak to full viper and red circle speak to the half snake. Wallace tree has three stages:

1. Increase each piece in multiplier with the same piece position of multiplicand. The created fractional items having distinctive weights Depending on the position of the multiplier bits .

2. The layers of the full adders and half adders are utilized for decreasing the quantity of halfway items to two.

3. After second step we get two lines of total and convey, include these lines with customary adders.

Clarification of second step:

For whatever length of time that there are more than two lines with the same weight include a taking

Array layer:

1. on the off chance that any three columns with the same weights take them and info them into a full snake. The outcome will put away in a yield line of the same weight that is aggregate and a yield line with a higher weight for each of the three info wires that is convey.

2. Take the two lines of the same weight left, enter them into a half viper.

3. In the event that there is only one line left, then it will interface with the following layer.

The Wallace tree has the numerous points of interest is that there are just O(log n) decrease layers (levels), and every layer has O(1) engendering delay. As making the incomplete items is O(1) and the last expansion is O(log n), the increase is just O(log n), very little slower than expansion (be that as it may, the entryway tally is more costly). It require O(log n2) time For including incomplete items with customary adders.

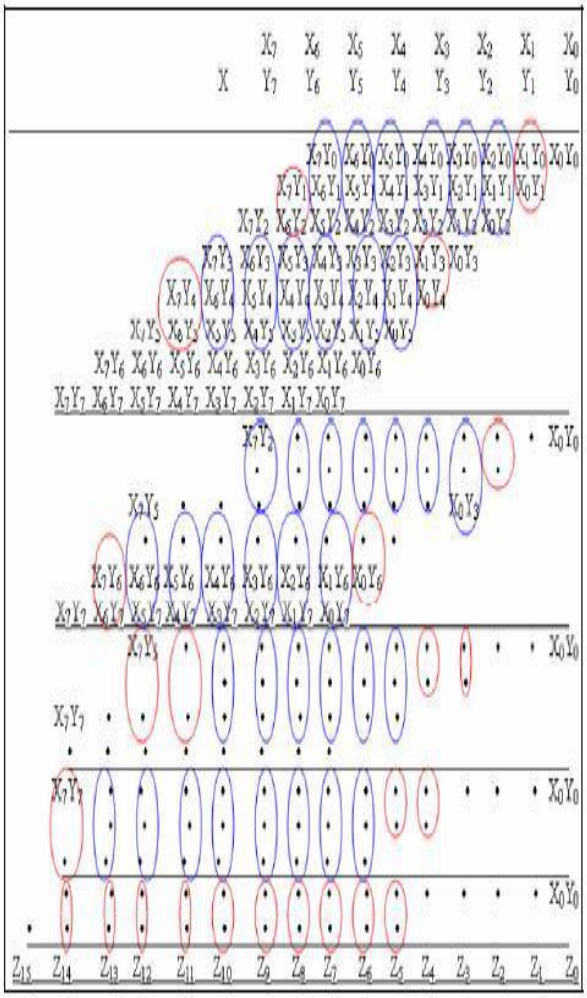

Fig.4.6 bit×6 bit Wallace tree multiplier.

Array Multiplier:

Array multiplier is well known because of its regular structure. Multiplier circuit are basically based shifting procedure and the repeted additions. the partial products are generated by performing multiplication in which the multiplier digit multiply with the multiplicand digit. The partial product is shifted based on their bit sequences and then added. The addition can be performed by normal carry propagation adder. If we have N no. of multiplier bits then we require N-1 adders.

Sequential Multiplier:

The multiplicand X has n bits and multiplier Y has m bits using single n-bit adder connected in sequence, this sequence circuit processes single partial products at a time then cycle circuit into m times . This type of circuit is called sequential multiplier. Sequential multipliers are more attractive for the low area requirement. The multiplication process is divided into some sequential steps in this sequence multiplier. In every step the generated partial products are added to an accumulated partial sum and the sum will of next steps. Therefore, each step of a sequential multiplication generates the partial products by performing three different operations, adding the generated partial products are added

to the accumulated partial sum and then shifting the partial sum. Figure 5 shows partial product generation and addition in a sequential multiplier.

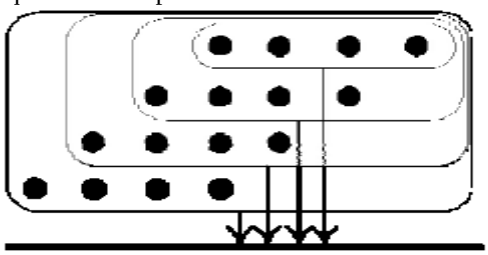

Fig.5.Row by row addition in a sequential multiplier.

C.Carry Save Adder

The fundamental reason for convey spare snake to diminishes the expansion of number. The spread deferral depends on the quantity of bits. The convey spare snake comprise of n full adders, every full viper produces aggregate and convey bits for a given inputs.

The whole entirety is ascertained by moving the convey arrangement left by one place and affixing a 0 to the front (most noteworthy piece) of the incomplete aggregate grouping and including this consequence of succession with RCA produces the subsequent n+1 bit esteem.

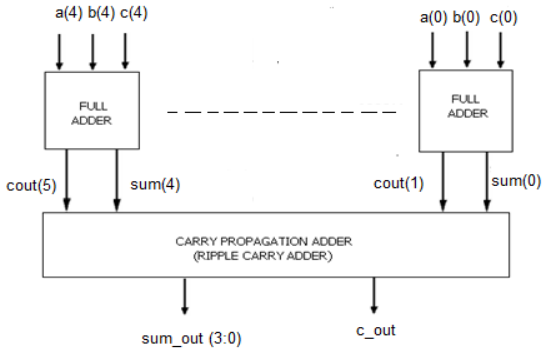

Fig.6.4-bit Carry Save Adder.

Basically, carry save adder is used for calculating the sum of three or more n-bit binary numbers. Carry save adder is like a full adder. As shown in the Fig. 6, here we are computing sum of two 4-bit binary numbers, so we take 4 full adders at first stage. Carry save unit consists of 4 full adders, each full adder consists of sum and carry based on the given input. Let X and Y are two 4-bit numbers and produces partial sum and carry as shown in the below :

Si = Xi xor Yi ; Ci = Xi and Yi

The final addition is then computed as:

1. Shifting the carry sequence C left by one place.
2. Placing a 0 to the front (MSB) of the partial sum sequence S.
3. Finally,a ripple carry adder is used to add these two together and computing the resulting sum.

Carry Save Adder Computataion :

X: 1 0 0 1 1
Y: 1 1 0 0 1
Z: + 0 1 0 1 1
S: 0 0 0 0 1
C: + 1 1 0 1 1
SUM: 1 1 0 1 1 1

In this outline 126 piece convey spare viper is utilized following the yield of the multiplier is 126 bits (2N). The primary motivation behind the is utilized to diminish the expansion from three numbers to two numbers. The spread postponement is 3gates regardless of the quantity of bits. The convey spare snake contains n full adders, processing a solitary total and conveys bits taking into account the given three piece number information. The whole aggregate can be figured by moving the convey succession left by one spot and afterward attaching a 0 to most noteworthy piece of the fractional entirety arrangement. Presently the fractional whole arrangement is included with swell convey unit bringing about n + 1 bit esteem. Where the do starting with one stage and specifically bolstered then onto the next. This procedure is proceeded without including any middle of the road convey spread. Since the representation of 126 piece convey spare snake is infeasible, thus a run of the mill 6 bit convey spare viper is appeared in the figure 3.Here we are registering the whole of two 126 piece paired numbers, then 126 half adders at the principal stage rather than 126 full snake. In this manner , convey spare unit contains 126 half adders, each of which processes single total and convey bit construct just with respect to the comparing bits of the two information numbers.Fig.7.Bit carry save adder.

If x and y are supposed to be two 126 bit numbers then it produces the partial products and carry as S and C respectively.

$$S_i = x_i \, 1\backslash \, y_i \qquad (4)$$

$$C_i = x_i \& y_i \qquad (5)$$

In the addition of two numbers without carry propagation performing addition by using the half adder and two ripple carry adders, the delay in that device is equal to the number full adders delay. all the output values are produced parallel in the carry save adder , resulting and then it takes less time than ripple carry adder . the accumulators uses parallel in parallel out processes

D.Carry Select Adder

A convey select viper is characterized into segments, each of which – with the exception of the slightest noteworthy –performs two increments in parallel, one expecting a convey in of zero, the other a convey in of one. The convey select is composed by utilizing the two four piece swell convey adders. on the off chance that we add two convey select viper then it performs options twice, one time with the suspicion of the convey being zero and the other expecting one.

Estimation of aggregate convey of the swell convey adders then they chose with the multiplexer once for the right convey is coming or not. The configuration schematic of Carry Select Adder is appeared in Fig. 6.

The convey select viper comes in the class of restrictive whole snake. Contingent entirety snake takes a shot at some condition. Aggregate and convey are computed by expecting information convey as 1 and 0 earlier the data convey comes. At the point when real convey information arrives, the real

ascertained estimations of entirety and convey are chosen utilizing a multiplexer.

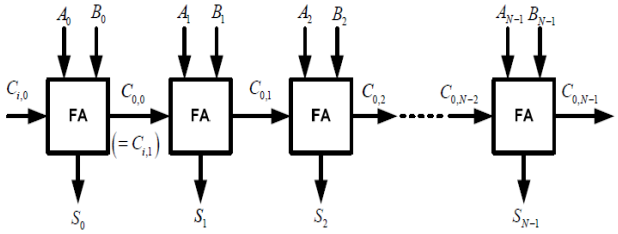

Fig.7. The N-bit Ripple Carry Adder constructed by N set single bit Full-adder

III.RESULTS

Schematics:

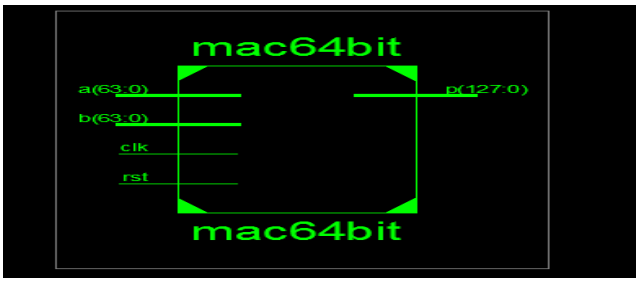

Fig.8. RTL Schematics of MAC64 bit

RTL Schematics:

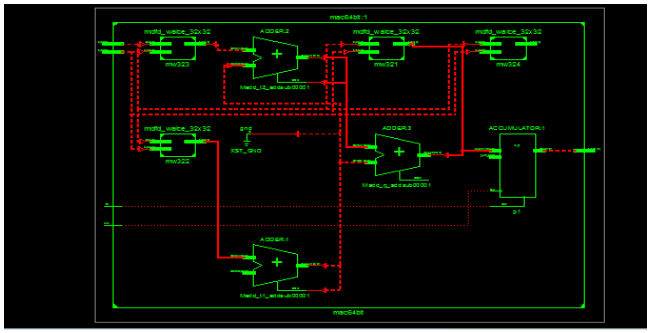

Fig.9. RTL Schematics of internal modules of MAC64 bit

Waveforms:

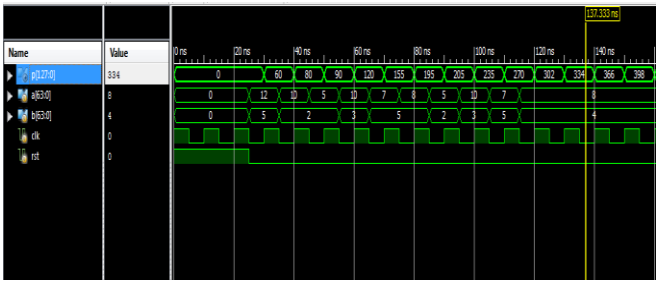

Fig.10.Outwavwforms of MAC64bit

IV.CONCLUSION

The Design of elite 64 bit Multiplier-and-Accumulator(MAC) was executed in this paper. The aggregate MAC unit works at a recurrence of 215 MHz's with an aggregate force scattering of 155.532 mW. Since the postponement of 64 bit MAC is less, this configuration can be utilized as a part of the framework which requires superior in processors including huge number of bits of the operation. The usefulness of the MAC is checked utilizing XILINX ISE 12.3i and combined utilizing XILINX synthesizer.

REFERENCES

[1].B.Cope,P.Cheung,W.Luk,andL.Howes,"PerformanceComparison of GraphicsProcessors to Reconfigurable Logic: ACase Study," IEEE Trans. Computers, vol. 57, no. 4, pp. 433-446,Apr. 2010.

[2] S. Dikmese, A. Kavak, K. Kucuk, S. Sahin, A. Tangel, and H. Dincer,"Digital Signal Processor against Field Programmable Gate ArrayImplementations of Space-Code CorrelatorBeamformer for SmartAntennas," IET Microwaves, Antennas Propagation, vol. 4, no. 5,pp. 573-577, May 2010.

[3] S. Roy and P. Banerjee, "An Algorithm for Trading off QuantizationError with Hardware Resources for MATLAB-based FPGA Design,"IEEE Trans. Computers, vol. 54, no. 5, pp. 666-676, July 2005.

[4] F. Schneider, A. Agarwal, Y.M. Yoo, T. Fukuoka, and Y. Kim,"A Fully Programmable Computing Architecture for MedicalUltrasoundMachines,"IEEE Trans.Information Technology inBiomedicine, vol. 14, no. 2, pp. 536-540, Mar. 2010.

[5] J. Hill, "The Soft-Core Discrete-Time Signal Processor Peripheral[Applications Corner]," IEEE Signal Processing Magazine, vol. 26,no. 2, pp. 112-115, Mar. 2007.